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ACADEMIC PROJECTS 2026-2027

ELECTRONICS & COMMUNICATIONS

- Embedded Systems
- VLSI / FPGA Design
- IoT Applications
- Wireless Communication
- Image / Signal Processing
- Antenna Design
- Robotics & Automation

& many more domains

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VLSI TITLE LIST 2026-27

S.No	Project Code	Title / Objective / Tools	Domain
1	TVMAFE828	**Power Efficient Multiplier Design for Error Resilient Edge Applications** **Objective:** Edge devices require low-power and efficient hardware for real-time computing applications. This project proposes a power-efficient approximate multiplier using an optimized 4:2 compressor to reduce power consumption and hardware complexity. The proposed design improves area and energy efficiency while maintaining acceptable accuracy for error-resilient applications. **Tools:** Xilinx Vivado	**Digital VLSI / Approximate Computing**
2	TVMAFE826	**scaleTRIM: Scalable TRuncation-Based Integer Approximate Multiplier with Linearization and Compensation** **Objective:** This project proposes a scalable approximate multiplier using truncation and linearization techniques to simplify multiplication operations. A LUT-based compensation mechanism is used to improve accuracy while reducing hardware complexity. The proposed architecture is evaluated for power, area, delay, and computational efficiency. **Tools:** Xilinx Vivado	**Digital VLSI / Approximate Computing**
3	TVMAFE824	**AMPEREISH: Approximate Multipliers for Power Efficiency in FPGA Designs Using Internal-Self-Healing** **Objective:** This project presents an FPGA-based approximate multiplier using the Internal-Self-Healing methodology for error-resilient applications. The proposed design improves power efficiency and FPGA resource utilization while maintaining acceptable computational accuracy. Performance is evaluated based on power, delay, area, and throughput. **Tools:** Xilinx Vivado	**Digital VLSI / FPGA Design**
4	TVMAFE822	**Efficient Approximate Recursive Multipliers (EARM) for Area and Power Optimized Image Processing Applications** **Objective:** This project develops scalable recursive approximate multipliers for image processing applications. The proposed architecture minimizes area, power consumption, and propagation delay while maintaining high computational accuracy. The design is validated through ASIC synthesis and performance comparison.	**Digital VLSI / Approximate Computing**

		Tools: Xilinx Vivado	
5	TVMAFE820	**Energy-Efficient Izhikevich Neuron Design Using Approximate CORDIC-Based Multipliers for Low-Power Neuromorphic Hardware** **Objective:** This project implements an energy-efficient Izhikevich neuron using approximate CORDIC-based multipliers for neuromorphic systems. The design replaces complex multiplication with shift-add operations to reduce power and hardware resources. The implementation is evaluated for energy efficiency, area, and computational performance. **Tools:** Xilinx Vivado	**Digital VLSI / Neuromorphic Computing**
6	TVMAFE819	**Impact of MAC Unit Design Architectures and Their Applications in Modern Computing** **Objective:** This project analyzes different Multiply-Accumulate (MAC) architectures used in AI, DSP, and high-performance computing applications. The study compares throughput, power consumption, area, and computational efficiency. The objective is to identify optimized MAC architectures for modern digital systems. **Tools:** Xilinx Vivado	**Digital VLSI / MAC Architecture**
7	TVMAFE818	**C-SIMD: CORDIC-Driven SIMD Processing Element for Resource-Efficient Multi-Precision Deep Learning Inference** **Objective:** This project proposes a configurable CORDIC-driven SIMD processing element for multi-precision deep learning inference. The architecture supports dynamic precision with optimized MAC operations to improve hardware utilization and throughput. The proposed design is evaluated for power, area, and inference performance. **Tools:** Xilinx Vivado	**Digital VLSI / AI Hardware Accelerator**
8	TVMAFE817	**An Edge-FPGA-Based Graph Convolutional Network Accelerator with FP8 Approximate Multipliers** **Objective:** This project develops an FPGA-based Graph Convolutional Network accelerator using FP8 approximate multipliers. The proposed architecture improves energy efficiency while maintaining high inference accuracy for edge AI applications. Performance is evaluated in terms of FPGA utilization, speed, and power consumption. **Tools:** Xilinx Vivado	**Digital VLSI / FPGA Accelerator**

9	TVMAFE816	**High-Performance Ternary Approximate Multiplier Designs with Stage-Wise Optimization for Low PDP and High Accuracy** **Objective:** This project presents optimized ternary approximate multipliers for error-resilient digital applications. The proposed architecture reduces power-delay product while maintaining high computational accuracy using optimized arithmetic stages. The design is analyzed for power, area, delay, and performance. **Tools:** Xilinx Vivado	**Digital VLSI / Approximate Computing**
10	TVMAFE815	**Accuracy-configurable Segmentation-based Approximate Multiplier for Error-resilient Edge-AI Applications** **Objective:** This project proposes a hardware-efficient segmentation-based approximate multiplier for resource-constrained Edge-AI applications. The design balances computational accuracy with reduced power, area, and hardware complexity using optimized approximation techniques. The proposed architecture is evaluated for FPGA and ASIC implementations based on power consumption, area utilization, and computational performance. **Tools:** Xilinx Vivado	**Digital VLSI / Approximate Computing**
11	TVMAFE814	**LUT-based Energy-efficient Approximate Multiplier for More Sustainable Neural Network Applications** **Objective:** This project proposes an LUT-based approximate multiplier to reduce power consumption in neural network applications. The design minimizes hardware complexity while improving energy efficiency through lookup table-based error compensation. The proposed architecture is evaluated for power, area, delay, and accuracy in AI workloads. **Tools:** Xilinx Vivado	**Digital VLSI / Approximate Computing**
12	TVMAFE813	**Design of an Area-Efficient and Low-Power 4:2 Approximate Compressor with Improved Image Quality Metrics** **Objective:** This project develops a low-power and area-efficient 4:2 approximate compressor using simplified logic optimization. The proposed design improves image quality while reducing power consumption and propagation delay. Performance is evaluated using hardware, error, and image quality metrics. **Tools:** Xilinx Vivado	**Digital VLSI / Approximate Computing**

13	TVMAFE812	**An Accuracy-and-Efficiency-Configurable Blade-Type Approximate Multiplier with Genetic Algorithm-Based Automatic Training Framework** **Objective:** This project presents a configurable blade-type approximate multiplier for AI and image processing applications. A genetic algorithm-based training framework is used to optimize accuracy and hardware efficiency. The proposed design is analyzed for power, area, delay, and approximation accuracy. **Tools:** Xilinx Vivado	**Digital VLSI / Approximate Computing**
14	TVMAFE810, TVMAFE811	**Design of a High-Density, Low-Power Parallel Prefix Approximate Adder** **Objective:** This project designs a high-density parallel prefix approximate adder with an efficient error reduction unit. The proposed architecture reduces power consumption and silicon area while maintaining computational accuracy. Performance is evaluated in terms of power, delay, area, and error metrics. **Tools:** Xilinx Vivado	**Digital VLSI / Approximate Adder Design**
15	TVMAFE809	**High-Speed MAGIC-Based Exact and Approximate Adders for In-Memory Computing** **Objective:** This project develops high-speed MAGIC-based exact and approximate adders for in-memory computing applications. The proposed architecture reduces memory access latency and energy consumption while supporting efficient arithmetic operations. The design is evaluated for speed, power, area, and computational performance. **Tools:** Cadence, Tanner	**Memory Design / In-Memory Computing**
16	TVMAFE851	**Analytical Error Evaluation and Hardware Implementation of Approximate Negation Circuits** **Objective:** This project investigates approximate negation circuits for improving energy efficiency in arithmetic systems. The proposed design reduces hardware complexity while maintaining acceptable computational accuracy for signed arithmetic operations. Performance is analyzed using power, delay, area, and error evaluation metrics. **Tools:** Xilinx Vivado	**Digital VLSI / Approximate Computing**
17	TVPGFE353	**A Reconfigurable Low-Latency Posit MAC Unit with Mixed Presicion** **Objective:** This project develops a reconfigurable low-latency Posit MAC unit supporting mixed-precision arithmetic. The proposed architecture	**Digital VLSI / MAC Architecture**

		improves numerical accuracy while reducing hardware latency and power consumption. The design is evaluated for throughput, area, and computational efficiency. **Tools:** Xilinx Vivado	
18	TVPGFE354	**A RISC-V Based Image Acquisition System Using CIS for Industrial Print Quality Inspection** **Objective:** This project implements a RISC-V based image acquisition system using a Contact Image Sensor for industrial inspection. The proposed system provides efficient image capture, processing, and transmission with low hardware cost. Performance is evaluated for speed, reliability, and real-time image acquisition. **Tools:** Xilinx Vivado	**Digital VLSI / RISC-V Architecture**
19	TVMAFE846	**Application and Assessment of FPGA-Based Filtering Algorithms for Enhancing Measurement Accuracy and Reliability in Greenhouse Monitoring Systems** **Objective:** This project implements FPGA-based filtering algorithms to improve measurement accuracy in greenhouse monitoring systems. The proposed design integrates multiple filtering techniques for reliable signal processing and reduced computational delay. The system is evaluated for accuracy, resource utilization, and real-time performance. **Tools:** Xilinx Vivado	**Digital VLSI / FPGA Design**
20	TVPGFE340	**A Novel Image Cryptosystem for FPGA Based on 8-bit Pseudorandom Number Generator with Enhanced Chaos and SHA-256** **Objective:** This project develops an FPGA-based image cryptosystem using an enhanced chaotic pseudorandom number generator and SHA-256. The proposed architecture provides secure image encryption with low hardware overhead and real-time performance. The design is evaluated for security, speed, power consumption, and FPGA resource utilization. **Tools:** Xilinx Vivado	**Digital VLSI / FPGA Security**
21	TVPGFE349	**Design and Implementation of a Fixed-Point FFT/IFFT Processor for NTRU Lattices** **Objective:** This project develops a 64-bit fixed-point FFT/IFFT processor optimized for NTRU lattice-based cryptography. The proposed architecture improves computational efficiency using optimized memory	**Digital VLSI / DSP Architecture**

		scheduling and twiddle factor compression. The design is evaluated for speed, hardware utilization, and cryptographic performance. **Tools:** Xilinx Vivado	
22	TVPGFE351	**High-Performance Posit Arithmetic for Accelerating Big Data Using Machine Learning Algorithm with Highly Pipelined Architecture in Breast Cancer Identification** **Objective:** This project implements a highly pipelined posit arithmetic architecture to accelerate machine learning algorithms for breast cancer detection. The proposed design improves computational speed and classification accuracy while reducing hardware complexity. The architecture is evaluated for throughput, latency, and prediction performance. **Tools:** Xilinx Vivado	**Digital VLSI / AI Hardware Accelerator**
23	TVMAFE847	**BIST Architecture for Multiple RAMs in SoC** **Objective:** This project develops a Built-In Self-Test (BIST) architecture for testing multiple RAM blocks in System-on-Chip designs. The proposed architecture performs parallel memory testing to reduce test time while improving fault coverage. The implementation is evaluated for hardware overhead, reliability, and testing efficiency. **Tools:** Cadence, Tanner	**Memory Design / Built-In Self-Test (BIST)**
24	TVPGFE356	**Vulnerability Assessment of Matter Protocol** **Objective:** This project analyzes the security vulnerabilities of the Matter protocol used in IoT and smart home applications. The proposed work evaluates authentication, communication, and key management mechanisms against common cyberattacks. The assessment aims to improve protocol security and ensure reliable device communication. **Tools:** Xilinx Vivado	**Digital Systems / IoT Security**
25	TVPGFE350	**Enhanced Functional Verification Models that Ensure the Full Functionality of an A-PLL Device** **Objective:** This project develops reusable functional verification models for Analog Phase-Locked Loop (A-PLL) devices using modern verification methodologies. The proposed framework improves verification coverage and accelerates mixed-signal design validation. The implementation is evaluated for verification efficiency and functional correctness.	**Analog Mixed Signal / Functional Verification**

		Tools: QuestaSim	
26	TVMABE873	**A Low-Power CMOS-Based Multiple and Variable Reference Voltage Generator Circuit** **Objective:** This project designs a low-power CMOS-based reference voltage generator capable of producing multiple stable voltage levels. The proposed circuit minimizes power consumption while maintaining high accuracy under process and temperature variations. The design is evaluated for voltage stability, power efficiency, and analog circuit performance. **Tools:** Cadence, Tanner	**Analog Mixed Signal / Voltage Reference Circuits**
27	TVPGFE346, TVPGFE345, TVPGFE347	**CNTFET-Based Hybrid Approximate Multiplier Design with Optimized Compressors for Error-Resilient Image Processing and Enhanced Power-Delay Efficiency** **Objective:** This project develops a CNTFET-based hybrid approximate multiplier using optimized compressor circuits for image processing applications. The proposed design reduces power-delay product while maintaining acceptable computational accuracy. The architecture is evaluated for power, delay, area, and image processing performance. **Tools:** Cadence, Tanner	**Nanoelectronics / CNTFET-Based VLSI**
28	TVPGFE355	**VLSI Design of Symmetric Two-Dimensional Finite Impulse Response Filter Architecture Using Approximate Circuits and Parallel Processing** **Objective:** This project designs a symmetric 2-D FIR filter architecture using approximate arithmetic and parallel processing techniques. The proposed architecture reduces hardware complexity while improving throughput and energy efficiency. The design is evaluated for FPGA resource utilization, power consumption, and filtering performance. **Tools:** Xilinx Vivado	**Digital VLSI / Digital Signal Processing (DSP)**
29	TVPGFE342, TVPGFE343	**Architectural and FPGA-Aware Optimizations of Vedic Multipliers for Approximate Computing** **Objective:** This project implements FPGA-optimized Vedic multipliers using approximate computing techniques for AI and image processing applications. The proposed architecture reduces hardware resource utilization and dynamic power while maintaining acceptable computational accuracy. Performance is evaluated in terms of area, power, delay, and FPGA efficiency.	**Digital VLSI / FPGA Design**

		Tools: Xilinx Vivado	
30	TVPGFE352	**Partial Encryption-Based Shamir Secret Sharing for Low-Latency and Secure Networks** **Objective:** This project proposes a partial encryption-based Shamir Secret Sharing scheme for secure and low-latency communication networks. The proposed method improves data security while reducing encryption delay and computational overhead. The implementation is evaluated for security, throughput, and communication efficiency. **Tools:** Xilinx Vivado	**Digital Systems / Hardware Security**
31	TVMAFE821	**Real-time Agricultural Image Securing System: A Selective Encryption-Based Approach on Edge Devices** **Objective:** This project proposes a selective image encryption framework for securing real-time agricultural images on edge devices. The design combines 2D-DWT and AES encryption to reduce computational overhead while maintaining data security. The proposed system is evaluated for encryption efficiency, execution time, and security performance. **Tools:** MATLAB	**Image Processing / Edge Computing / Cryptography**
32	TVMAFE823	**A High-Capacity Image Steganography Based on Random Separate Hashing Data Structure with Secure CHACHA20-DRBG and AES Encryption Algorithms** **Objective:** This project develops a secure image steganography technique using hashing, ChaCha20-DRBG, and AES encryption. The proposed method increases data embedding capacity while preserving image quality and security. Performance is evaluated based on embedding capacity, imperceptibility, and resistance to steganalysis attacks. **Tools:** MATLAB	**Image Processing / Information Security**
33	TVMAFE825	**Latency-Optimal Quantum Circuits for IoT Networks** **Objective:** This project focuses on designing latency-optimized quantum circuits for next-generation IoT communication systems. The proposed approach minimizes circuit delay while balancing energy efficiency, programmability, and hardware cost. The design is analyzed for latency, quantum circuit depth, and communication performance. **Tools:** Xilinx Vivado, MATLAB	**Quantum Computing / IoT Hardware**

34	TVMAFE827	**Quantum Overflow Detection for Reliable Bioinspired Image Enhancement** **Objective:** This project develops a quantum overflow detection circuit for reliable biomedical image enhancement. The proposed design utilizes quantum computing principles to improve image processing accuracy and computational efficiency. Performance is validated through quantum simulation and hardware implementation. **Tools:** Xilinx Vivado, MATLAB	**Quantum Computing / Image Processing**
35	TVMAFE829	**Programmable Clock Distribution Using Switching Matrices for Field Programmable Gate Arrays** **Objective:** This project proposes a programmable clock distribution network using switching matrices for FPGA devices. The architecture improves clock routing flexibility while minimizing clock skew and propagation delay. The proposed design is evaluated for routing efficiency, timing performance, and resource utilization. **Tools:** Xilinx Vivado	**Digital VLSI / FPGA Architecture**
36	TVMAFE830	**Securing RISC-V SoC With Random Clock Self Complementary Countermeasure** **Objective:** This project develops a secure RISC-V SoC by integrating an AES hardware accelerator with a Random Clock Self Complementary countermeasure. The proposed architecture protects against power analysis attacks while maintaining low hardware overhead. Performance is evaluated in terms of security, power consumption, and hardware efficiency. **Tools:** Xilinx Vivado	**Digital VLSI / RISC-V Architecture**
37	TVMABE816	**Compact GaN MMIC Doherty Power Amplifier Module Employing Phase-Reduced Load Modulation Network** **Objective:** This project presents a compact GaN MMIC Doherty Power Amplifier with an optimized load modulation network. The proposed design improves power-added efficiency, gain, and linearity while reducing circuit size. Performance is evaluated for modern wireless communication applications. **Tools:** Cadence, Tanner	**RF & Microwave / Power Amplifier Design**
38	TVMABE831	**A 3-bit Digitally-Reconfigurable Driving-Capability nW-Powered Three-Stage Fully-Synthesizable Inverter-Based OTA for Multi-Load Applications**	**Analog Mixed Signal / OTA Design**

		Objective: This project develops a digitally reconfigurable ultra-low-power inverter-based OTA for multi-load applications. The proposed architecture adapts drive capability while minimizing power consumption and maintaining stable operation. The design is analyzed for gain, power efficiency, and load-driving performance. **Tools:** Cadence, Tanner	
39	TVMABE823	**CMOS 90nm Based Two Stage Differential Amplifier** **Objective:** This project designs a two-stage differential amplifier using 90nm CMOS technology for analog integrated circuits. The proposed amplifier provides high gain, good common-mode rejection, and low power consumption. The design is evaluated for gain, bandwidth, stability, and power performance. **Tools:** Cadence, Tanner	**Analog Mixed Signal / CMOS Analog Design**
40	TVMABE824	**A High-Gain Ultra Low Power Subthreshold OTA Using Three Distributed Positive-Feedback Paths** **Objective:** This project presents a high-gain, ultra-low-power subthreshold OTA using distributed positive-feedback paths. The proposed architecture enhances voltage gain and transconductance while operating with very low power consumption. The design is evaluated for gain, power dissipation, and analog signal processing performance. **Tools:** Cadence, Tanner	**Analog Mixed Signal / OTA Design**
41	TVMABE835	**A Linear Ultralow Flicker Noise Switched-Transconductance Downconversion Mixer** **Objective:** This project develops a switched-transconductance downconversion mixer with ultra-low flicker noise for RF receiver applications. The proposed architecture improves conversion gain while reducing thermal noise and power consumption. The design is evaluated for noise figure, linearity, and high-frequency performance. **Tools:** Cadence, Tanner	**Analog Mixed Signal / RF Mixer Design**
42	TVMABE837	**Voltage Scaling Analysis of a Single-Tail Dynamic Comparator Circuit** **Objective:** This project designs a high-speed single-tail dynamic comparator for low-power mixed-signal applications. The proposed architecture minimizes delay and dynamic power while maintaining fast and reliable decision making. The design is analyzed for voltage scaling, power consumption, and comparator performance.	**Analog Mixed Signal / Comparator Design**

		Tools: NGSpice	
43	TVMABE839	**A 6.8 µA Quiescent Current, 200 mA Maximum Load Current, Capacitor-Less NMOS LDO for Sensor Applications** **Objective:** This project presents an ultra-low-power capacitor-less NMOS LDO regulator for portable sensor applications. The proposed design achieves low quiescent current, fast transient response, and stable voltage regulation over varying loads. Performance is evaluated based on power efficiency, load regulation, and stability. **Tools:** Cadence, Tanner	**Analog Mixed Signal / LDO Regulator**
44	TVMABE840	**Control-Oriented Modeling of Comparator Overdrive Delay for Stabilizing High-Frequency Current-Mode DC-DC Converters** **Objective:** This project develops a control-oriented model for comparator overdrive delay in high-frequency DC-DC converters. The proposed approach enhances converter stability by reducing current-sensing interference and subharmonic oscillations. The design is evaluated for transient response, stability, and converter performance. **Tools:** NGSpice	**Power Electronics / DC-DC Converter**
45	TVMABE842	**A Ka-Band Time-Modulated Phase-Invariant Variable-Gain Amplifier With 30-dB Gain Tuning Based on Duty-Cycle Control** **Objective:** This project designs a Ka-band variable-gain amplifier with wide gain tuning using duty-cycle control techniques. The proposed architecture maintains phase invariance while improving gain linearity and reducing power consumption. The amplifier is evaluated for high-frequency wireless communication performance. **Tools:** Cadence, Tanner	**Analog Mixed Signal / RF Amplifier Design**
46	TVMABE843	**Irradiation of a Radiation Hard Charge Amplifier for Neutron Diagnostics** **Objective:** This project develops a radiation-hardened charge amplifier for reliable neutron detection in harsh environments. The proposed design improves radiation tolerance while maintaining accurate signal amplification and long-term reliability. Performance is evaluated for nuclear, space, and particle detection applications. **Tools:** NGSpice	**Analog Mixed Signal / Radiation-Hardened Circuits**

47	TVMABE845	**Improved Dynamic Range Charge-Sensitive Amplifier** **Objective:** This project presents a charge-sensitive amplifier with enhanced dynamic range for precision signal detection. The proposed design improves linearity, minimizes electronic noise, and enhances charge conversion accuracy. The amplifier is evaluated for radiation sensing and imaging system applications. **Tools:** Cadence, Tanner	**Analog Mixed Signal / Charge Amplifier**
48	TVMABE847	**220 GHz, 8.5-dBm Saturated Output Power Wideband Power Amplifier in SiGe BiCMOS** **Objective:** This project develops a 220-GHz wideband power amplifier using SiGe BiCMOS technology for terahertz communication systems. The proposed design provides high output power, wide bandwidth, and improved power efficiency. Performance is analyzed for high-frequency wireless and sensing applications. **Tools:** Cadence, Tanner	**RF & Microwave / Power Amplifier Design**
49	TVMABE848	**Design and Analysis of a 1.5-mW Ka-Band CMOS Quadrature VCO Using Self-Forward-Bias and AC-Floating Body Topology** **Objective:** This project designs a low-power Ka-band CMOS Quadrature Voltage-Controlled Oscillator using self-forward-bias techniques. The proposed architecture improves phase noise, frequency stability, and power efficiency for high-frequency communication systems. The design is evaluated for oscillation performance and low-power operation. **Tools:** NGSpice	**Analog Mixed Signal / VCO Design**
50	TVMABE853 / TVMABE854D / TVMABE855D	**A 91 nW Static Power and Ultra-Low Noise Subthreshold CMOS 65nm Operational Amplifier for Sensor Applications** **Objective:** This project develops an ultra-low-power CMOS operational amplifier operating in the subthreshold region for sensor applications. The proposed design minimizes static power consumption while achieving low input noise and sufficient gain. The amplifier is evaluated for biomedical, IoT, and environmental monitoring systems. **Tools:** Cadence, Tanner	**Analog Mixed Signal / Operational Amplifier Design**
51	TVMABE858	**Design for Slew-Rate in Multi-Stage CMOS OTAs** **Objective:** This project focuses on improving the slew rate of multi-stage CMOS operational transconductance amplifiers for high-speed analog applications. The proposed design enhances large-signal response while	**Analog Mixed Signal / OTA Design**

		maintaining high gain, stability, and low power consumption. The OTA is evaluated for slew rate, settling time, and overall analog performance. **Tools:** Cadence, Tanner	
52	TVMABE815	**A High-Gain Ultra-Low-Power Subthreshold OTA Using Three Distributed Positive-Feedback Paths** **Objective:** This project develops a high-gain subthreshold OTA using distributed positive-feedback paths for ultra-low-power operation. The proposed architecture improves voltage gain and transconductance while minimizing power consumption. The design is evaluated for gain, power efficiency, and sensor interface applications. **Tools:** Cadence, Tanner	**Analog Mixed Signal / OTA Design**
53	TVMABE817	**A Low-Power, High-Stability CMOS Bandgap Reference With Post-Regulation for Wearable IoT Applications** **Objective:** This project designs a CMOS bandgap reference with post-regulation to provide a stable reference voltage for wearable IoT devices. The proposed architecture improves temperature stability and line regulation while minimizing power consumption. The design is analyzed for voltage stability, power efficiency, and reliability. **Tools:** Cadence, Tanner	**Analog Mixed Signal / Bandgap Reference**
54	TVMABE819	**Accurate Closed-Form Delay Formulas for Interconnected CMOS Gates Based on First-Order Thresholded Hybrid Systems** **Objective:** This project develops accurate delay estimation models for interconnected CMOS gates using first-order thresholded hybrid systems. The proposed analytical method improves timing prediction while reducing computational complexity. The design is evaluated for delay accuracy and VLSI timing analysis performance. **Tools:** Xilinx Vivado	**Digital VLSI / Timing Analysis**
55	TVMABE822	**A Fully Integrated Multiphase CMOS Charge-Pump Harvester With Self-Biased Blocking Network** **Objective:** This project presents a CMOS charge-pump energy harvester with a self-biased blocking network for low-voltage energy harvesting. The proposed design enhances power conversion efficiency while minimizing reverse charge leakage. Performance is evaluated for energy harvesting efficiency and portable IoT applications. **Tools:** Cadence, Tanner	**Analog Mixed Signal / Energy Harvesting**

56	TVMABE828	**AND-Logic Embedded 7T SRAM-Based Backplane Circuit for Low-Power Micro-Displays** **Objective:** This project develops a 7T SRAM-based backplane circuit with embedded AND logic for low-power micro-display applications. The proposed architecture reduces area, power consumption, and circuit complexity while improving display control efficiency. The design is evaluated for memory reliability and energy-efficient display operation. **Tools:** Cadence, Tanner	**Memory Design / SRAM**
57	TVMABE834	**A 24–28 GHz Single-Chip GaN MMIC T/R Front-End Using Doherty Power Amplifier as Embedded Switches in Rx Mode** **Objective:** This project designs a compact GaN MMIC transmit/receive front-end operating in the 24–28 GHz frequency band. The proposed architecture integrates a Doherty power amplifier to improve efficiency while reducing insertion loss and chip area. Performance is evaluated for 5G millimeter-wave communication systems. **Tools:** Cadence, Tanner	**RF & Microwave / MMIC Design**
58	TVMABE841	**A Fast-Transient Capless LDO With Push-Pull Dynamic Capacitor Compensation for Wide Range of Capacitive Loads** **Objective:** This project develops a capacitorless LDO regulator with push-pull dynamic compensation for improved transient response. The proposed design ensures stable voltage regulation over a wide range of capacitive loads while minimizing power consumption. Performance is evaluated for load regulation, recovery time, and stability. **Tools:** Cadence, Tanner	**Analog Mixed Signal / LDO Regulator**
59	TVMABE846	**Compact Planar Balun for 915-MHz Push-Pull Power Amplifier** **Objective:** This project designs a compact planar balun for a 915-MHz push-pull power amplifier with low insertion loss. The proposed design improves impedance matching, phase balance, and amplifier efficiency while reducing circuit size. The balun is evaluated for RF communication and ISM band applications. **Tools:** Cadence, Tanner	**RF & Microwave / Passive RF Design**
60	TVMABE856	**A High-Gain, Low-Voltage Operational Amplifier With Bias-Stress and PVT Robustness for Large-Area Temperature Sensing on LTPS Substrates** **Objective:** This project develops a high-gain, low-voltage operational amplifier with improved robustness against bias-stress and PVT	**Analog Mixed Signal / Operational Amplifier Design**

		variations. The proposed design ensures reliable performance while maintaining low power consumption and high accuracy. The amplifier is evaluated for flexible electronics and temperature sensing applications. **Tools:** Cadence, Tanner	
61	TVMABE859	**A 1-V, 6.93-nW Subthreshold Source-Follower Biopotential LPF with Combined Gain Compensation and Current Cancellation in 65-nm CMOS** **Objective:** This project develops an ultra-low-power biopotential low-pass filter using subthreshold CMOS technology for biomedical applications. The proposed design improves signal accuracy through gain compensation and current cancellation while minimizing power consumption. The filter is evaluated for noise performance, energy efficiency, and wearable healthcare applications. **Tools:** Cadence, Tanner	**Analog Mixed Signal / Biomedical Circuits**
62	TVMABE874/ TVMABE822/ TVMABE821	**A Fully Integrated Multiphase CMOS Charge-Pump Harvester with Self-Biased Blocking Network** **Objective:** This project designs a multiphase CMOS charge-pump energy harvester for efficient low-voltage energy conversion. The proposed architecture reduces reverse charge leakage while improving output voltage and power conversion efficiency. The design is evaluated for self-powered IoT, wearable, and wireless sensor applications. **Tools:** Cadence, Tanner	**Analog Mixed Signal / Energy Harvesting**
63	TVMABE863	**Design and Characterization of CMOS Differential Pair Circuits for Membership Function Generation with Noise Analysis in Fuzzy Logic Systems** **Objective:** This project develops CMOS differential pair circuits for accurate membership function generation in fuzzy logic systems. The proposed design improves linearity while reducing power consumption and analyzing circuit noise effects. Performance is evaluated for intelligent control and low-power decision-making applications. **Tools:** NGSpice	**Analog Mixed Signal / Fuzzy Logic Circuits**
64	TVMABE868	**A 65 nm Radiation-Hardened CAM Design and Evaluation for Space Applications** **Objective:** This project designs a radiation-hardened content addressable memory using 65-nm CMOS technology for space applications. The proposed architecture improves reliability by mitigating radiation-induced	**Memory Design / CAM**

		faults while maintaining high-speed search capability. The design is evaluated for power efficiency, fault tolerance, and aerospace computing systems. **Tools:** NGSpice	
65	TVMABE869	**A 6.8–14-GHz Ring-Based Sampling-PLL Achieving 69.3-fs Jitter Under 50-mV Supply Noise** **Objective:** This project develops a ring-based sampling PLL with ultra-low timing jitter for high-speed communication systems. The proposed design enhances supply-noise immunity while improving phase noise and clock stability. Performance is evaluated for RF transceivers and mixed-signal integrated circuits. **Tools:** Cadence, Tanner	**Analog Mixed Signal / PLL Design**
66	TVMABE870	**A 3–20 V High-Voltage LDO With User-Defined 1.25–19.6 V Output and 1.5-A Load Capability** **Objective:** This project designs a programmable high-voltage LDO regulator with high current-driving capability for power management applications. The proposed architecture provides accurate output regulation, fast transient response, and excellent thermal stability. The design is evaluated for industrial, automotive, and programmable power supply systems. **Tools:** Cadence, Tanner	**Analog Mixed Signal / LDO Regulator**
67	TVMAFE831	**Deterministic Dual-Role I2C Verification via Bus Ownership Invariants and Bounded Runtime Switching** **Objective:** This project develops a verification framework for dual-role I2C interfaces capable of dynamic master-slave switching. The proposed methodology ensures safe bus ownership while preventing deadlocks and protocol violations during runtime transitions. The verification environment is evaluated for functional correctness and protocol reliability. **Tools:** QuestaSim	**Digital VLSI / Verification (SystemVerilog/UVM)**
68	TVMAFE832	**A Low-Power, High-Throughput Multimode FFT Processor Incorporating the ASPC Algorithm** **Objective:** This project develops a low-power multimode FFT processor supporting multiple transform sizes for DSP applications. The proposed architecture improves throughput while reducing hardware complexity	**Digital VLSI / DSP Architecture**

		and power consumption. Performance is evaluated for FPGA and ASIC implementations in communication and AI systems. **Tools:** Xilinx Vivado	
69	TVMAFE833	**Knowledge Graph-Guided LLMs for Generating Secure Verilog Code of Finite State Machine in SoCs** **Objective:** This project develops a knowledge graph-guided framework for generating secure Verilog code for finite state machines. The proposed approach enhances code security by identifying vulnerabilities and applying secure design patterns during code generation. The framework is evaluated for secure SoC design and hardware code generation accuracy. **Tools:** Xilinx Vivado	**Digital VLSI / Hardware Security & FSM Design**
70	TVMAFE834	**Generation of Synthesizable Verilog Code from Natural Language Specifications** **Objective:** This project develops a framework to generate synthesizable Verilog code directly from natural language specifications using large language models. The proposed approach ensures syntactic correctness through automated compilation, simulation, and synthesis verification. The framework is evaluated for code accuracy, synthesizability, and hardware design efficiency. **Tools:** QuestaSim	**Digital VLSI / HDL Automation & AI**
71	TVMAFE835	**An Educational Platform for Web-Based Simulation and Visualization of RISC-V Processor Architectures** **Objective:** This project develops a web-based platform for simulation and visualization of RISC-V processor architectures. The proposed system helps users understand single-cycle, multi-cycle, and pipelined processor designs through interactive learning. The platform is evaluated for usability, functionality, and educational effectiveness. **Tools:** Xilinx Vivado	**Digital VLSI / RISC-V Architecture**
72	TVMAFE872	**Scalable Network-on-Chip Design for FPGA Implementation** **Objective:** This project develops a scalable Network-on-Chip framework for automatic FPGA implementation. The proposed architecture generates synthesizable Verilog code for multiple NoC topologies while reducing design complexity. Performance is evaluated based on scalability, routing efficiency, and FPGA resource utilization. **Tools:** Xilinx Vivado	**Digital VLSI / Network-on-Chip (NoC)**

73	TVMAFE873	**Machine Learning-Driven Prediction of Optimal Design Parameters for Ripple Carry Adder** **Objective:** This project applies machine learning techniques to predict optimal design parameters for ripple carry adders. The proposed approach improves power, delay, and area optimization while reducing VLSI design time. The model is evaluated for prediction accuracy and design efficiency. **Tools:** Xilinx Vivado	**Digital VLSI / AI for VLSI Design**
74	TVMAFE838	**A Reconfigurable Built-In Self-Test Scheme for the Evaluation Circuits of Digital SRAM-IMC Architectures** **Objective:** This project develops a reconfigurable built-in self-test scheme for digital SRAM-based in-memory computing architectures. The proposed method improves fault detection while simplifying testing of inaccessible evaluation circuits. Performance is evaluated for test coverage, reliability, and hardware overhead. **Tools:** NGSpice	**Memory Design / SRAM & BIST**
75	TVMAFE839	**FPGA-Based Real-Time ECG Classification System Using Quantized Inception-ResNeXt Neural Network and CWT Approximation** **Objective:** This project develops a real-time ECG classification system on FPGA using a quantized neural network architecture. The proposed design improves classification accuracy while minimizing hardware resources and power consumption. Performance is evaluated for real-time inference, accuracy, and FPGA efficiency. **Tools:** Xilinx Vivado	**Digital VLSI / FPGA & AI Accelerator**
76	TVMAFE840	**Energy-Efficient Logarithmic Floating-Point Multipliers Using Truncation-Based Error Compensation for Fault-Tolerant Applications** **Objective:** This project develops energy-efficient logarithmic floating-point multipliers using truncation-based error compensation techniques. The proposed architecture reduces hardware cost while maintaining acceptable computational accuracy. The design is evaluated for power, area, delay, and fault-tolerant performance. **Tools:** Xilinx Vivado	**Digital VLSI / Approximate Computing**
77	TVMAFE841	**FPGA-Based Low-Power Signed Approximate Multipliers for Diverse Error-Resilient Applications**	**Digital VLSI / FPGA & Approximate Computing**

		Objective: This project designs FPGA-friendly signed approximate Booth multipliers for low-power error-resilient applications. The proposed architecture reduces hardware complexity while improving resource utilization and computational efficiency. Performance is evaluated based on power, FPGA utilization, and multiplication accuracy. **Tools:** Xilinx Vivado	
78	TVMAFE842	**Memory-Optimized Block Compression for High-Speed Memory Testing** **Objective:** This project develops a memory-optimized block compression technique for high-speed memory testing. The proposed method reduces test vector storage requirements while improving testing flexibility and efficiency. The design is evaluated for compression ratio, memory utilization, and testing performance. **Tools:** Cadence, Tanner	**Memory Design / Memory Testing**
79	TVMAFE843	**FPGA-Based FP8 Approximate Neural Network Engine** **Objective:** This project develops an FPGA-based FP8 approximate neural network engine for low-power AI inference. The proposed architecture replaces multiplication with efficient approximation techniques to reduce hardware complexity and energy consumption. The design is evaluated for inference accuracy, FPGA resource utilization, and power efficiency. **Tools:** Xilinx Vivado	**Digital VLSI / FPGA & AI Accelerator**
80	TVMAFE844	**Modified and Optimized Architecture for 16-Bit Signed Magnitude Adder Using Carry Look-Ahead Adder on FPGA** **Objective:** This project develops an optimized 16-bit signed magnitude adder using a Carry Look-Ahead architecture for FPGA implementation. The proposed design improves arithmetic speed while reducing delay and hardware complexity. Performance is evaluated based on FPGA resource utilization, power, and timing efficiency. **Tools:** Xilinx Vivado	**Digital VLSI / FPGA & Arithmetic Circuits**
81	TVMAFE845	**Optimizing High-Level Synthesis Sparse Matrix-Vector Kernel for Alveo FPGAs** **Objective:** This project optimizes a sparse matrix-vector multiplication kernel using high-level synthesis for Alveo FPGA platforms. The proposed architecture improves memory access efficiency and computational throughput through hardware-aware optimization	**Digital VLSI / FPGA & High-Level Synthesis**

		techniques. The design is evaluated for execution speed, FPGA utilization, and power efficiency. **Tools:** Xilinx Vivado, Vivado HLS	
82	TVMABE875	**A Ring-Oscillator-Based Digital Harmonic-Mixing Fractional-N PLL** **Objective:** This project develops a digital harmonic-mixing fractional-N PLL using a ring oscillator for high-speed clock generation. The proposed architecture reduces phase noise and locking time while improving frequency resolution and power efficiency. Performance is evaluated for communication and System-on-Chip applications. **Tools:** Cadence, Tanner	**Analog Mixed Signal / PLL Design**
83	TVMABE877	**An Ultra-Low-Jitter Sampling-Filter-Based Charge-Pump PLL With Resistive-Discharge Time-Amplifying Phase-Frequency Detector** **Objective:** This project designs an ultra-low-jitter charge-pump PLL with a sampling filter and enhanced phase-frequency detector. The proposed architecture improves synchronization accuracy while reducing phase noise and reference spurs. The design is evaluated for high-speed communication and mixed-signal systems. **Tools:** Cadence, Tanner	**Analog Mixed Signal / PLL Design**
84	TVMABE871	**High-Precision Hybrid CMOS/MTJ BGR With Improved Temperature Coefficient and Reduced Area** **Objective:** This project develops a hybrid CMOS/MTJ bandgap reference with improved temperature stability and reduced silicon area. The proposed design provides an accurate reference voltage while maintaining low power consumption and robustness against PVT variations. Performance is evaluated for precision analog and mixed-signal applications. **Tools:** Cadence, Tanner	**Analog Mixed Signal / Bandgap Reference**
85	TVMABE873/ TVMABE832	**A Low-Power CMOS-Based Multiple and Variable Reference Voltage Generator Circuit** **Objective:** This project designs a low-power CMOS reference voltage generator capable of producing multiple adjustable voltage levels. The proposed architecture improves voltage accuracy and stability while minimizing power dissipation and chip area. The design is evaluated for power management and analog integrated circuit applications. **Tools:** Cadence, Tanner	**Analog Mixed Signal / Voltage Reference**

86	TVMABE820	**A 1.2-ns Delay Level Shifter Circuit Using Multiple Fast Charging, Discharging, and Feed-Forward Paths** **Objective:** This project develops a high-speed level shifter with multiple charging, discharging, and feed-forward paths for fast voltage conversion. The proposed design minimizes propagation delay while maintaining reliable operation across different voltage domains. Performance is evaluated for speed, power consumption, and level conversion efficiency. **Tools:** Cadence, Tanner	**Analog Mixed Signal / Level Shifter**
87	TVMABE827	**A Complementary Positive Feedback-Assisted Current Mirror-Based Level Shifter for Energy-Efficient Level Conversion for Wide Voltage Ranges** **Objective:** This project presents an energy-efficient current mirror-based level shifter with complementary positive feedback for wide voltage operation. The proposed architecture reduces power consumption while improving switching speed and voltage conversion reliability. The design is evaluated for low-power VLSI and mixed-voltage SoC applications. **Tools:** Cadence, Tanner	**Analog Mixed Signal / Level Shifter**
88	TVMABE830	**A 1 Grad TID-Tolerant Bandgap Voltage Reference for HEP Applications in 28 nm CMOS Node** **Objective:** This project develops a radiation-hardened bandgap voltage reference for high-energy physics applications using 28-nm CMOS technology. The proposed design maintains stable reference voltage under extreme radiation and PVT variations. Performance is evaluated for radiation tolerance, temperature stability, and long-term reliability. **Tools:** Cadence, Tanner	**Analog Mixed Signal / Bandgap Reference**
89	TVMABE836	**A 2.1µA 1.65V-to-5V Supply 10ppm/°C Bandgap Reference with Source-Degenerated Piecewise Curvature Compensation** **Objective:** This project develops an ultra-low-power bandgap reference with piecewise curvature compensation for accurate voltage generation. The proposed design improves temperature stability, line regulation, and power efficiency over a wide supply range. The circuit is evaluated for analog and mixed-signal power management applications. **Tools:** Cadence, Tanner	**Analog Mixed Signal / Bandgap Reference**
90	TVMABE838	**A 400 V High-Speed Level-Shifting Gate Driver with Adaptive Signal-Path Disconnection for 278 V/ns dv/dt Immunity in Soft-Switching Converters**	**Analog Mixed Signal / Gate Driver**

		Objective: This project develops a high-speed 400 V level-shifting gate driver with adaptive signal-path disconnection for improved dv/dt immunity. The proposed design minimizes switching errors while ensuring reliable signal transmission in high-voltage converters. Performance is evaluated for propagation delay, noise immunity, and power efficiency. **Tools:** Cadence, Tanner	
91	TVMABE844	**A Comprehensive Survey of Custom Layout Techniques for 6T, 8T, and 10T SRAM Bitcells Across Planar CMOS and FinFET Technology Nodes** **Objective:** This project analyzes custom layout techniques for SRAM bitcells across CMOS and FinFET technologies. The study evaluates area, power, stability, and leakage characteristics of different SRAM architectures. The comparison helps identify efficient layout strategies for advanced memory design. **Tools:** Cadence, Tanner	**Memory Design / SRAM**
92	TVMABE850	**A High-Gain Ultra-Low-Power Subthreshold OTA Using Three Distributed Positive-Feedback Paths** **Objective:** This project designs a high-gain subthreshold OTA using distributed positive-feedback paths for ultra-low-power operation. The proposed architecture improves gain and transconductance while maintaining low energy consumption. Performance is evaluated for analog signal processing and biomedical applications. **Tools:** Cadence, Tanner	**Analog Mixed Signal / OTA**
93	TVMABE851	**A K-Band CMOS Variable-Gain Phase Shifter Using an Impedance-Invariant Vector-Summing Amplifier With Adaptive Bleeding Currents** **Objective:** This project develops a K-band CMOS variable-gain phase shifter using an impedance-invariant vector-summing amplifier. The proposed design improves gain control, phase accuracy, and power efficiency for RF communication systems. Performance is evaluated for high-frequency wireless applications. **Tools:** Cadence, Tanner	**Analog Mixed Signal / RF Circuit Design**
94	TVMABE857	**A Non-Uniform Current-Starved Ring Oscillator Ising Machine With Unidirectional Coupling Circuit for Combinatorial Problems Solving**	**Analog Mixed Signal / Oscillator & AI Hardware**

		Objective: This project develops a ring oscillator-based Ising machine for solving combinatorial optimization problems efficiently. The proposed architecture improves convergence accuracy while reducing power consumption and hardware complexity. Performance is evaluated for AI acceleration and optimization applications. **Tools:** Cadence, Tanner	
95	TVMABE860	**A Physically Unclonable Function With Less Than 4.16E–7 BER Featuring Secure In-Cell HCI Burn-In and nMOS-Dominant PUF Data Generation** **Objective:** This project develops a highly reliable Physically Unclonable Function (PUF) for secure hardware authentication. The proposed design minimizes bit error rate while improving key generation reliability under PVT variations. The circuit is evaluated for hardware security and IoT applications. **Tools:** Cadence, Tanner	**Hardware Security / Physically Unclonable Function (PUF)**
96	TVMABE861	**Power-Efficient Three-Stage Dynamic Comparator for Wide Input Common-Mode Range** **Objective:** This project develops a power-efficient three-stage dynamic comparator with a wide input common-mode range. The proposed design reduces delay and power consumption while maintaining high comparison accuracy. Performance is evaluated for ADCs and mixed-signal integrated circuits. **Tools:** Cadence, Tanner	**Analog Mixed Signal / Comparator**
97	TVMABE862	**Low-Noise Multipath Amplifier With Slew-Rate Boosting and Ping-Pong Auto-Zero** **Objective:** This project designs a low-noise multipath amplifier with slew-rate boosting and auto-zero techniques. The proposed architecture reduces offset and noise while improving settling time and signal accuracy. Performance is evaluated for precision analog and biomedical applications. **Tools:** Cadence, Tanner	**Analog Mixed Signal / Amplifier Design**
98	TVMABE864	**Noise Modulation of a Bandgap Reference by Using a Single Resistor** **Objective:** This project develops a low-noise bandgap reference using a single-resistor noise modulation technique. The proposed design improves voltage stability while reducing output noise and power consumption.	**Analog Mixed Signal / Bandgap Reference**

		Performance is evaluated for precision analog and power management circuits. **Tools:** Cadence, Tanner	
99	TVMABE865	**Pseudo-Dynamic AOI and OAI Standard-Cell-Based Comparators** **Objective:** This project develops pseudo-dynamic AOI and OAI standard-cell-based comparators for high-speed digital applications. The proposed architecture reduces propagation delay and power consumption while maintaining compatibility with standard-cell design flows. Performance is evaluated for ADCs, processors, and SoC designs. **Tools:** Cadence, Tanner	**Analog Mixed Signal / Comparator**
100	TVMABE866	**Universal-Gate-Driven Efficient 3-D Vedic Multiplier Designs for Nanoscale Logic Systems With Application of High-Performance Computing** **Objective:** This project designs a universal-gate-based 3-D Vedic multiplier for nanoscale logic systems. The proposed architecture reduces power, delay, and hardware complexity while improving computational efficiency. Performance is evaluated for high-performance computing, DSP, and AI accelerator applications. **Tools:** Xilinx Vivado	**Digital VLSI / Vedic Multiplier**

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6-2-85/B, Old Maternity Hospital Road, Thyagaraja Nagar,
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+91 90303 33433 | 0877 2261612

www.takeoffprojects.com | info@takeoffprojects.com | /takeoffedugroup