takeoff
A Division of Youngminds Technologies (P) Ltd

2015 – 2016 (M.TECH) IEEE VLSI PROJECT TITLES

PROJECT NUMBER	TITLE	DOMAIN
1	Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic	Arithmetic
2	A Modified Partial Product Generator for Redundant Binary Multipliers	Arithmetic
3	Design & Analysis of 16 bit RISC ProcessorUsing low Power Pipelining	Arithmetic
4	Design and Analysis of Approximate Compressors for Multiplication	Arithmetic
5	Design and Implementation of 16 x 16 MultiplierUsing Vedic Mathematics	Arithmetic
6	Design and implementation of fast floating point multiplier unit	Arithmetic
7	Area and frequency optimized 1024 point Radix-2 FFT processor on FPGA	Arithmetic
8	Design and Simulation of Single Layered Logic Generator Block using Quantum Dot Cellular Automata	Arithmetic
9	Design of area and power aware reduced Complexity Wallace Tree multiplier	Arithmetic
10	Design of area and power efficient digital FIR filter using modified MAC unit	Arithmetic
11	Design of low power and high speed Carry Select Adder using Brent Kung adder	Arithmetic
12	Energy-Efficient Approximate Multiplication for Digital Signal Processing and Classification Applications	Arithmetic
13	FPGA implementation of scalable microprogrammed FIR filter architectures using Wallace tree and Vedic multipliers	Arithmetic
14	FPGA implementation of vedic floating point multiplier	Arithmetic

15	FPGA realization and performance evaluation of fixed-width modified Baugh-Wooley multiplier	Arithmetic
16	High-Speed and Energy-Efficient Carry Skip AdderOperating Under a Wide Range ofSupply Voltage Levels	Arithmetic
17	FPGA Based Scalable Fixed Point QRD Core Using Dynamic Partial Reconfiguration	Arithmetic
18	Intelligent and Adaptive Traffic Light Controllerusing FPGA	Arithmetic
19	Low-Cost High-Performance VLSI Architecture for Montgomery Modular Multiplication	Arithmetic
20	Novel Reconfigurable Hardware Architecture for Polynomial MatrixMultiplications	Arithmetic
21	A High-Speed FPGA Implementation of an RSD-Based ECC Processor	Arithmetic
22	Analysis of ternary multiplier using booth encoding technique	Arithmetic
23	A Novel Quantum-Dot Cellular Automata X-bit x 32-bit SRAM	Arithmetic
24	HMFPCC - Hybrid-mode floating point conversion co-processor	Arithmetic
25	On the Analysis of Reversible Booth's Multiplier	Arithmetic
26	Pre-Encoded Multipliers Based on Non-Redundant Radix-4 Signed-Digit Encoding	Arithmetic
27	Reverse Converter Design via Parallel-Prefix Adders Novel Components, Methodology, andImplementations	Arithmetic
28	Revisiting Central Limit Theorem Accurate Gaussian Random Number Generation in VLSI	Arithmetic
29	Advanced low power RISC processor design using MIPS instruction set	Arithmetic
30	RTL implementation for AMBA ASB APB protocol at system on chip level	Arithmetic

31	Run-time reconfigurable multi-precision floating point multiplier design for high speed, low-power applications	Arithmetic
32	Technology optimized fixed-point bit-parallel multiplier for LUT based FPGAs	Arithmetic
33	Truncated ternary multipliers	Arithmetic
34	An efficient floating point multiplier design for high speed applications using Karatsuba algorithm and Urdhva-Tiryagbhyam algorithm	Arithmetic
35	A Combined SDC-SDF Architecture for Normal-IO Pipelined Radix-2 FFT	Digtal Signal Processing
36	A High-Performance FIR Filter Architecture forFixed and Reconfigurable Applications	Digtal Signal Processing
37	An Efficient VLSI Architecture of a ReconfigurablePulse-Shaping FIR Interpolation FilterforMultistandard DUC	Digtal Signal Processing
38	Obfuscating DSP Circuits via High-LevelTransformations	Digtal Signal Processing
39	Razor Based Programmable Truncated Multiply and Accumulate, Energy-Reduction for Efficient Digital Signal Processing	Digtal Signal Processing
40	Fully Reused VLSI Architecture of FM0Manchester Encoding Using SOLS Technique for DSRC Applications	Communication
41	FPGA implementation of an advanced encoding and decoding architecture of polar codes	Communication
42	Fault Tolerant Parallel Filters Based on Error Correction Codes	Communication
43	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks	Communication
44	A novel VHDL implementation of UART with single error correction and double error detection capability	Communication

45	A Low-Complexity Multiple Error CorrectingArchitecture Using Novel Cross ParityCodes Over GF*(2m)*	Communication
46	A Fault Detection and Tolerance Architecture for Post-Silicon Skew Tuning	Communication
47	A Class of SEC-DED-DAEC Codes Derived From Orthogonal Latin Square Codes	Communication
48	VLSI Implementation of a Key Distribution Server Based Data Security Scheme for RFID System	Communication
49	Optimized approach of sobel edge detection technique using Xilinx system generator	Communication
50	PAQCS Physical Design-Aware Fault-Tolerant Quantum Circuit Synthesis	Communication
51	Glitch free combinational clock gating approach in nanometer VLSI circuits	Low Power
52	Low power compressor based MAC architecture for DSP applications	Low Power
53	Low power multiplier architectures using vedic mathematics in 45nm technology for high speed computing	Low Power
54	Low-Cost Multiple Bit Upset Correction inSRAM-Based FPGA Configuration Frames	Low Power
55	Power Optimization of Communication System Using Clock Gating Technique	Low Power
56	Low-Power Programmable PRPG With Test Compression Capabilities	Low Power
57	Design and synthesis of bandwidth efficient QPSK modulator for low power VLSI design	Low Power
58	A Sub-mW, Ultra-Low-Voltage, Wideband Low-Noise Amplifier Design Technique	Low Power

59	Frequency-Tuning Negative-Conductance Boosted Structure and Applications for Low-Voltage Low-Power Wide-Tuning-Range VCO	Low Power
60	TM-RF Aging-Aware Power-Efficient Register File Design for Modern Microprocessors	Low Power
61	A novel realization of reversible LFSR for its application in cryptography	Testing
62	Preemptive Built-In Self-Test for In-Field Structural Testing	Testing
63	Scan Chain Masking for Diagnosis of Multiple Chain Failures in a Space Compaction Environment	Testing
64	Scan Test Bandwidth Management for Ultralarge-Scale System-on-Chip Architectures	Testing
65	Multiplexer based High Throughput S-box for AES Application	Testing
66	Skewed-Load Test Cubes Based on Functional Broadside Tests for a Low-Power Test Set	Testing
67	A Method of One-Pass Seed Generationfor LFSR-Based Deterministic/Pseudo-Random Testing of Static Faults	Testing
68	Built-in Self-Calibration and Digital-Trim Techniquefor 14-Bit SAR ADCs Achieving ±1 LSB INL	Testing
69	Optimized approach of sobel edge detection technique using Xilinx system generator	Imageprocessing
70	Reconfigurable architecture of adaptive median filter — An FPGA based approach for impulse noise suppression	Imageprocessing
71	High efficiency VLSI implementation of an edge-directed video up-scaler using high level synthesis	Imageprocessing
72	Voltage mode implementation of highly accurate analog multiplier circuit	Back-End

73	Low-power, high-speed dual moduluspresca lers based on branch-merged true single-phase clocked scheme	Back-End
74	Low Power Multiplier Architectures Using VedicMathematics in 45nm Technology for High SpeedComputing	Back-End
75	Digtial to time converter using SET	Back-End
76	Design of high speed ternary full adder and threeinput XOR circuits using CNTFETs	Back-End
77	Design Method of Single-Flux-QuantumLogic Circuits Using Dynamically Reconfigurable Logic Gates	Back-End
78	Design and simulation of single layered Logic Generator Block using Quantum Dot Cellular Automata	Back-End
79	Design and Performance Evaluation of ALow Transistor Ternary CNTFET SRAM Cell	Back-End
80	A 0.25-V 28-nW 58-dB Dynamic Range Asynchronous Delta Sigma Modulator in 130-nm Digital CMOS Process	Back-End
81	A 0.325 V, 600-kHz, 40-nm 72-kb 9T Sub threshold SRAM with Aligned Boosted Write Word line and Negative Write Bit line Write-Assist	Back-End
82	A High Speed 256-Bit Carry Look Ahead AdderDesign Using 22nm Strained Silicon Technology	Back-End
83	A Highly-Scalable Analog Equalizer Using a Tunable and Current-ReusableActive Inductor for 10-Gb/s I/O Links	Back-End
84	A Sub-mW, Ultra-Low-Voltage, Wideband Low-Noise Amplifier Design Technique	Back-End
85	An All-Digital Scalable and Reconfigurable Wide-Input Range Stochastic ADC Using Only Standard Cells	Back-End
86	Read Performance The Newest Barrier in Scaled STT-RAM	Back-End

87	On the Nonvolatile Performance of Flip-FlopSRAM Cells With a Single MTJ	Back-End
88	High-Performance and High-Yield 5 nm Underlapped FinFET SRAM Design usingP-type Access Transistors	Back-End
89	High-Frequency CMOS Active Inductor Design Methodology and Noise Analysis	Back-End
90	Efficient Static D-Latch Standard Cell Characterization Using a Novel Setup Time Model	Back-End
91	A CMOS PWM Transceiver Using Self-Referenced Edge Detection	Back-End
92	Achieving Power Reduction by using Multi-Bit Flip-Flop	Back-End
93	Implementation of a low-power Multi shaped CMOS Fuzzifier Circuit	Back-End
94	Design and FPGA Implementation of Optimized 32- Bit Vedic Multiplier and Square Architectures	Back-End

PROJECT SUPPORTS FOR STUDENTS:

- PROJECT ABSTRACT
- PROJECT IEEE BASE PAPER/ REFERENCE PAPER
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1	Generation and validation of multi operand carry save adders from the web	Arithmetic
2	A high speed floating point dot product unit	Arithmetic
3	Low power noise tolerant domino 1-bit full adder	Arithmetic
4	Design of Dedicated Reversible Quantum Circuitry for Square Computation	Arithmetic
5	Area–Delay–Power Efficient Carry-Select Adder	Arithmetic
6	Hardware acceleration with pipelined adder for Support Vector Machine classifier	Arithmetic
7	High speed convolution and deconvolution algorithm (Based on Ancient Indian Vedic Mathematics)	Arithmetic
8	A New Algorithm for Carry-Free Addition of Binary Signed-Digit Numbers	Arithmetic
9	4-2 Compressor Design with New XOR-XNOR Module	Arithmetic
10	Comparative performance analysis of XOR-XNOR function based high-speed CMOS full adder circuits	Arithmetic
11	Implementation of high speed low power combinational and sequential circuits using reversible logic	Arithmetic
12	Arithmetic-Based Binary-to-RNS Converter Modulo {2n ±k} for jn-Bit Dynamic Range	Arithmetic
13	Design and estimation of delay, power and area for Parallel prefix adders	Arithmetic
14	Low Voltage and Low Power 64-Bit Hybrid Adder Design Based on Radix-4 Prefix Tree Structure	Arithmetic
15	A Novel Parallel Multiplier for 2's Complement Numbers Using Booth's Recoding Algorithm	Arithmetic

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16	On the design of efficient modulo 2^n+1 multiply-add-add units	Arithmetic
17	A low-cost realization of quantum ternary adder using muthukrishnan-stroud gate	Arithmetic
18	Design and Analysis of Approximate Compressors for Multiplication	Arithmetic
19	Recursive Approach to the Design of a Parallel Self-Timed Adder	Arithmetic
20	Fast Radix-10 Multiplication Using Redundant BCD Codes	Arithmetic
21	A Modified Bec Logic Design of High Speed Csla For Low Power And Area Efficient Applications	Arithmetic
22	Delay Locked Loop Using Glitch Free Nand-Based DCDL	Arithmetic
23	Design and Implementation of Fast Addition Using QSD for Signed and Unsigned Numbers	Arithmetic
24	Design and Implementation of Floating Point Multiplier Using Wallace and Dadda Algorithm	Arithmetic
25	Design of High Speed Low Power Multiplier Using Nikhilam Sutra with Help of Reversible Logic	Arithmetic
26	Design of High Speed, Area Efficient, Low Power Vedic	Arithmetic
27	FPGA Implementation of Single Precision Floating Point Multiplier using High Speed Compressors	Arithmetic
28	Double Precision IEEE-754 Floating-Point Adder Design Based on FPGA	Arithmetic
29	Design of High Speed Multiplier using Vedic Mathematics	Arithmetic
30	Design and FPGA implementation of compressor based VEDIC multiplier	Arithmetic

31	Low Power 64bit Multiplier Design by Vedic Mathematics	Arithmetic
32	Design of Efficient Graph Based Algorithm with Modified Carry save Adder	Arithmetic
33	Design of Floating Point Arithmetic Logic Unit with Universal Gate	Arithmetic
34	Design Of Reversible Fault TOLERENT Decoder Using MOS Transistors	Arithmetic
35	Design Of Low Power / High Speed Multiplier Using Spurious Power Suppression Technique (SPST)	Arithmetic
36	An Efficient High Speed Wallace Tree Multiplier	Arithmetic
37	Implementation Of Unsigned Multiplier Using Modified CSLA	Arithmetic
38	Design and Analysis of Conventional CMOS and Energy Efficient Adiabatic Logic for Low Power VLSI Application	Arithmetic
39	Design of high speed, area efficient, low power Vedic Multiplier using Reversible logic Gates	Arithmetic
40	Design of High Performance 64 bit MAC Unit	Arithmetic
41	A New High Performance Logic Style for Arithmetic Circuits	Arithmetic
42	A novel approach to realize built-in-self-test (BIST) enabled UART using Verilog	Testing
43	Co-optimization of memory BIST grouping, test scheduling, and logic placement	Testing
44	Testing PUF-based secure key storage circuits	Testing
45	Built-in self-test for manufacturing TSV defects before bonding	Testing
46	Low-Power Programmable PRPG With Test Compression Capabilities	Testing

47	High Performance BIST PLL approach for VCO testing	Testing
48	Low cost fault detector guided by permanent faults at the end of FPGAs life cycle	Testing
49	Design and implementation of a BIST embedded inter-integrated circuit bus protocol over FPGA	Testing
50	1450.6.2-2014 - IEEE Standard for Memory Modeling in Core Test Language	Testing
51	Property-checking based LBIST for improved diagnosability	Testing
52	Built-in self-test (BIST) algorithm to mitigate process variation in millimeter wave circuits	Testing
53	Built-in self-test and characterization of polar transmitter parameters in the loop-back mode	Testing
54	Cross logic: A new approach for defect-tolerant circuits	Testing
55	Formal Verification and Debugging of Array Dividers with Auto-correction Mechanism	Testing
56	Scalable arithmetic cells for iterative logic array	Testing
57	A Low Transition Test Pattern Generation Of Multiple Sic Vectors Based On BIST Schemes	Testing
58	Test Pattern Generation Using BIST Schemes	Testing
59	Modified Hamming Codes to Enhance Short Burst Error Detection in Semiconductor Memories (Short Paper)	Communication
60	Biff (Bloom Filter) Codes: Fast Error Correction for Large Data Sets	Communication
61	Low Delay Single Symbol Error Correction Codes based on Reed Solomon Codes	Communication
62	Implementing Double Error Correction Orthogonal Latin Squares Codes in Xilinx FPGAsA Class of SEC-DED-DAEC Codes Derived From Orthogonal Latin Square Codes	Communication

63	Fault Tolerant Linear State Machines	Communication
64	Triple error detection for Imai-Kamiyanagi codes based on subsyndrome computations	Communication
65	Coding and Detection for Channels with Written-In Errors and Inter-Symbol Interference	Communication
66	Majority Logic Decoding Of Euclidean Geometry Low Density Parity Check (EG-LDPC) Codes	Communication
67	Design and Implementation of Orthogonal Code Convolution Using Enhanced Error Control Technique	Communication
68	Efficient FPGA and ASIC Realizations of a DA-Based Reconfigurable FIR Digital Filter	Communication
69	FPGA based partial reconfigurable fir filter design	Communication
70	Quaternary Logic Lookup Table in Standard CMOS	Communication
71	An Efficient VLSI Architecture of a Reconfigurable Pulse-Shaping FIR Interpolation Filter for Multistandard DUC	Communication
72	Design of parallel pipelined feed forward architecture for zero frequency & minimum computation (zmc) algorithm of FFT	Communication
73	Distributed Arithmetic Based Non Recursive Filter for High Throughput and Low Power Applications	Communication
74	FPGA design of high throughput STBC-OFDM system for low power applications	Communication
75	Low Power Fir Filter Design Using Truncated Multiplier	Communication
76	Low-power and low-area adaptive FIR	Communication
77	Reducing power and time in cache system using bloom filter under write through policy	Communication
78	VLSI Implementation of Fixed-Point LMS Adaptive Filter with Low Adaptation Delay	Communication
79	VLSI Implementation of Delayed LMS Adaptive Filter with Efficient Area-Power-Delay	Communication

80	Optimized adaptive FIR filter based on distributed arithmetic	Communication
81	Enhanced Pipelined Architecture for Adaptive FIR Filter Based on Distributed Arithmetic	Communication
82	Low Complexity Digit Serial FIR Filter By Multiple Constant Multiplication Algorithms	Communication
83	VLSI Architecture For Optimized Low Power Digit Serial FIR Filter With FPGA	Communication
84	A High Speed FFT/IFFT Processor For MIMO OFDM Systems	Communication
85	High Throughput In MIMO Wireless Communication Using Adaptive SVDENGINE Design	Communication
86	Reconfigurable Sequential Minimal Optimization Algorithm for High-Throughput MIMO-OFDM Systems	Communication
87	A Novel Approach For Designing A D-Flip Flop Using MTCMOS Technique For Reducing Power Consumption	Communication
88	Design And Implementation Of Lifting Based 2d Discrete Wavelet Transforming FPGA	Communication
89	Fast FIR Algorithm Based Area-Efficient Parallel FIR Digital Filter Structures	Communication
90	Analysis of Fast FIR Algorithms based Area Efficient FIR Digital Filters	Communication
91	A Novel Fast FIR Algorithm for Area-Efficient Parallel FIR Digital Filter Structures Utilizes Symmetric Convolutions	Communication
92	Design And Implementation Of An On-Chip Permutation Network For Multiprocessor System-On-Chip	Communication
93	Design Of An On-Chip Permutation Network For Multiprocessor Soc	Communication

94	Design and simulation of 16 Bit UART Serial Communication Module Based on Verilog	Communication
95	A Low Power Single Phase Clock Distribution Multiband Network	Communication
96	Design of Low Power L2 Cache Architecture Using Way Tag Information	Communication
97	Glitch free NAND based Digitally Controlled Delay Line for Spread Spectrum Clock Generator	Communication
98	Design and Implementation of Runtime Reconfigurable High Resolution Digital Pulse Width Modulator on FPGA	Communication
99	Design of Clocked Pair Shared Flip Flop Using low Power Techniques	Low Power
100	Power Reduction for Sequential Circuit using Merge Flip-Flop Technique	Low Power
101	Design of MERGABLE Flip-Flop for Low Power VLSI Circuits	Low Power
102	A Novel Approach to Reduce Clock Power by Using Multi Bit Flip Flops	Low Power
103	Achieving Power and Area Reduction by Redesigning Existing Memory IC	Low Power
104	Automated High-Level Synthesis of Low Power/Area Approximate Computing Circuits	Low Power
105	Design Flow for Flip-Flop Grouping in Data-Driven Clock Gating	Low Power
106	Adiabatic Technique for Power Efficient Logic Circuit Design	Low Power

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