takeoff
A Division of Youngminds Technologies (P) Ltd

2015 – 2016 (B.TECH)IEEEVLSI PROJECT TITLES

PROJECT NUMBER	TITLE	DOMAIN
1	Efficient Error Detection and Correction UsingDecimal Matrix Code for Memory Reliability	Communication
2	Reducing Dynamic Power Dissipation In LFSR Using LookAhead Clock Gating And Double Edge Triggering	Low Power
3	FPGA Based N-Bit LFSR To Generate RandomSequence Number	Testing
4	Implementation Of High Speed Low PowerVedic Multiplier Using Reversible Logic	Arithmetic
5	UART Serial Communication Module Design and SimulationBased on VHDL	Communication
6	Aging Effect Tolerant Multiprecision Razor-BasedMultiplier	Arithmetic
7	Merging of Test Cubes using Test Point Insertionfor Low-Power TestCompaction	Low Power
8	Radix-8 Modified Booth RecoderForHigh Speed Add-Multiply Operator	Arithmetic
9	Design of High Speed Multiplier Using Vedic MathematicsTechnique	Arithmetic
10	Convolution and Deconvolution Using VedicMathematics	Communication
11	Efficient Computing Techniques using VedicMathematics Sutras	Arithmetic
12	Design and Implementation of Partial Reconfigurable FirFilter Using Distributed Arithmetic Architecture	Digital Signal Processing
13	Design of Low Power Sequential System Using Multi Bit FLIPFLOP With Data Driven Clock Gating	Low Power
14	Realization of LMS Adaptive Algorithm UsingVerilogHdl For Low Complexity	Digital Signal Processing

15	Detection and Correction of Multiple Cell Upsets in Static RandomAccess Memories Using Decimal Matrix Code	Communication
16	Design of Floating Point Multiplier Using VedicMathematics	Arithmetic
17	Approximate Compressors for 32 X 32 BitMultiprecision Multipliers	Arithmetic
18	Error Detection and Correction in SRAM Cell Using DecimalMatrix Code	Communication
19	Performance Analysis Of Parallel Prefix Adder	Arithmetic
20	Improved Error Correction Capability using Parity Matrix Code	Communication
21	Analysis Of Various MCM Algorithms ForReconfigurableRrc Fir Filter	Digital Signal Processing
22	Design of ALU using reversible logic based LowPower Vedic Multiplier	Arithmetic
23	A Novel Method for Area Efficient N-Bit FullComparator Using Quantum-Dot CellularAutomata	Arithmetic
24	A Novel Approach for Parallel CRC Generation forHigh Speed Application	Communication
25	An Efficient Design and Implementation of ALU using GatedDiffusion Index	Back End
26	Reliability of Memory Storage System UsingDecimal Matrix Code and Meta-Cure	Communication
27	Simulation Analysis and Characterization of Low Power andHigh-Speed Digital Circuits	Low Power
28	On-Chip Comparison based Secure Output ResponseCompactor for Scan-based Attack Resistance	Testing
29	Reducing Power Consumption Using Clock GatingTechnique In Flipflop	Low Power

30	A Novel SOC Design Based on Multi-Bit Flip Flop Design for Reducing Area	Low Area
31	Review of LP-TPG Using LP-LFSR for Switching Activities	Testing
32	Design of reversible MAC unit, shift and addmultiplier using PSDRM technique	Arithmetic
33	Purpose of Low-Power Linear Feedback Shift Register (LFSR) byusing Bipartite and Random Injection Method for Low Power BIST	Testing
34	Implementation Of TestableReversible Sequential Circuit On FPGA	Testing
35	New VLSIBWA Architecture ForFinding The First WMaximum/Minimum Values UsingSorting Algorithms	Communication
36	VLSI Implementation of ALU using Reversible Logic with Vedic Mathematics	Arithmetic
37	Design Of Compact Reversible Low Power N-Bit BinaryComparator Using Reversible Gates	Arithmetic
38	Design A Low Power eight-bit Reversible ParallelBinary Adder/Subtractor	Arithmetic
39	Design of Low Power Optimized FilterArchitecture using VLSI Technique	Digital Signal Processing
40	Area optimization Technique for Multi-standard DUC	Digital Signal Processing
41	Design of Reversible Code Converters forQuantum Computer based Systems	Arithmetic
42	Design and FPGA Implementation of Optimized 32- Bit Vedic Multiplier and Square Architectures	Arithmetic

PROJECT SUPPORTS FOR STUDENTS:

- PROJECT ABSTRACT
- PROJECT IEEE BASE PAPER/ REFERENCE PAPER
- PROJECT PRESENTATION IN PPT FORMAT
- PROJECT REVIEW ASSISTANCE FOR VIVA
- PROJECT DIAGRAMS
- PROJECT SOURCE CODE
- PROJECT REPORT
- PROJECT SCREEN SHOTS
- PROJECT DEMO
- PROJECT EXPLANATION
- PLAGARISM DOCUMENTATION
- INTERNATIONAL JOURNAL/CONFERENCE PUBLISHING
- PROJECT ACCEPTANCE LETTER
- PROJECT COMPLETION CERTIFICATE

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PROJECT NUMBER	TITLE	DOMAIN
1	High Speed Convolution And Deconvolution Algorithm (Based On Ancient Indian Vedic Mathematics)	Arithmetic
2	8 Bit RISC Processor Using VERILOG HDL	Arithmetic
3	Implementation Of High Speed Low Power Combinational And Sequential Circuits Using Reversible Logic	Arithmetic
4	Design And Estimation Of Delay, Power And Area For Parallel Prefix Adders	Arithmetic
5	Design And Analysis Of Approximate Compressors For Multiplication	Arithmetic
6	A Modified BEC Logic Design Of High Speed CSLA For Low Power And Area Efficient Applications	Arithmetic
7	Design And Implementation Of Floating Point Multiplier Using Wallace And DADDA Algorithm	Arithmetic
8	Design Of High Speed Low Power Multiplier Using Nikhilam Sutra With Help Of Reversible Logic	Arithmetic
9	Design Of High Speed, Area Efficient, Low Power Vedic Multiplier using Reversible Logic Gate	Arithmetic
10	FPGA Implementation Of Single Precision Floating Point Multiplier Using High Speed Compressors	Arithmetic
11	Low Power 64bit Multiplier Design By Vedic Mathematics	Arithmetic
12	An Efficient High Speed Wallace Tree Multiplier	Arithmetic
13	Design Of High Performance 64 Bit Mac Unit	Arithmetic
14	A Low Transition Test Pattern Generation Of Multiple Sic Vectors Based On BIST Schemes	Testing
15	Test Pattern Generation Using BIST Schemes	Testing

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16	Modified Hamming Codes to Enhance Short Burst Error Detection in Semiconductor Memories (Short Paper)	Communication
17	An Efficient VLSI Architecture of a Reconfigurable Pulse-Shaping FIR Interpolation Filter for Multi Standard DUC	Digital Signal Processing
18	Low Power Fir Filter Design Using Truncated Multiplier	Arithmetic
19	Low Complexity Digit Serial FIR Filter By Multiple Constant Multiplication Algorithms	Digital Signal Processing
20	VLSI Architecture For Optimized Low Power Digit Serial FIR Filter With FPGA	Digital Signal Processing
21	Fast FIR Algorithm Based Area-Efficient Parallel FIR Digital Filter Structures	Digital Signal Processing
22	Analysis of Fast FIR Algorithms based Area Efficient FIR Digital Filters	Digital Signal Processing
23	A Novel Fast FIR Algorithm for Area-Efficient Parallel FIR Digital Filter Structures Utilizes Symmetric Convolutions	Digital Signal Processing
24	Design And Implementation Of An On-Chip Permutation Network For Multiprocessor System-On-Chip	Communication
25	Design Of An On-Chip Permutation Network For Multiprocessor SOC	Communication
26	Design and simulation of 16 Bit UART Serial Communication Module Based on Verilog	Communication
27	A Low Power Single Phase Clock Distribution Multiband Network	Communication
28	Enhanced Memory Reliability Using Parity Matrix Code	Communication
29	FPGA implementation of high speed 8 bit Vedic Multiplier using Fast adders	Arithmetic
30	Implementing Double Error Correction Orthogonal Latin Squares Codes In Xilinx FPGA	Communication
31	To Test Iscas-85 C432 27 By Using Built-In Generation Of Functional Broadside	Testing

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