FIR Filter Implementation using Modified Distributed Arithmetic Architecture

Abstract

In this project use Distributed Arithmetic (DA) technique for FIR filter. In this technique consist of Look Up Table (LUT), shift register and accumulator. Based on this technique multipliers in FIR filter are removed. Multiplication is performed through shift and addition operations. The LUT can be subdivided into a number of LUT to reduce the size of the LUT for higher order filter. Each LUT operates on a different set of filter taps. Analysis on the performance of various filter orders with different address length are done using Xilinx synthesis tool. The proposed architecture provides less latency and less area compared with existing structure of FIR filter.

Screen shot results

RTL schematic
Technology schematic

Output waveform

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