ACHIEVING REDUCED AREA BY MULTI-BIT FLIP FLOP DESIGN

Abstract

Timing Optimization is one of the most important objectives of the designer in the Modern VLSI world. Memory elements play a vital role on Digital World. The basic memory elements of designer considerations are Latch and flip flop. In this paper, we analyze the design of Single-bit Flip flop (SBFF) and made performance comparison over the Multi-bit Flip-flop (MBFF). For improving Flip flop performance one of the promising way is to merge the clock pulse. The Multi-bit Flip-flop is designed by single clock pulse and achieves same functionality like two single-bit Flip-flop. A shift register is designed using both Single-Bit Flip-Flop (SBFF) and Multi-Bit Flip-Flop (MBFF). This paper analyzes the timing performance of both SBFF and MBFF in Xilinx Virtex-5 family (XC5VLX50). These results in favor of Multi-Bit Flip-Flop as reduction of Clock network such as clock buffer and gate delay.

Screenshot results
PIPO output waveform