Area–Delay–Power Efficient Carry-Select Adder

Screenshot results

Block diagram:

![Block diagram of Area–Delay–Power Efficient Carry-Select Adder](image-url)
Technology Schematic:

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### Design summary:

#### Device Utilization Summary (estimated values):

<table>
<thead>
<tr>
<th>Logic Utilization</th>
<th>Used</th>
<th>Available</th>
<th>Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Slices</td>
<td>23</td>
<td>2440</td>
<td>0%</td>
</tr>
<tr>
<td>Number of LUTs</td>
<td>35</td>
<td>4360</td>
<td>8%</td>
</tr>
<tr>
<td>Number of IOBs</td>
<td>50</td>
<td>100</td>
<td>50%</td>
</tr>
</tbody>
</table>

#### Detailed Reports:

- **Synthesis Report**
  - Status: Current
  - Generated: Sat Nov 22 17:45:13 2014
  - Errors: 0
  - Warnings: 0
  - Infos: 0

- **Translation Report**
- **Map Report**
- **Place and Route Report**
- **Power Report**
- **Post-MP Static Timing Report**
- **Elaboration Report**

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Simulation Results:

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