takeoffedu GROUP
(A Division of Youngminds Technology Solutions Pvt.Ltd)
Your Destiny is Our Destiny

CERTIFIED ISO 9001:2015 COMPANY

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2018-2019 B.TECH VLSI IEEE TITLES

S.NO	TITLES
	FRONTEND
1.	Approximate Quaternary Addition with the Fast Carry Chains of FPGAs
2.	A Low-Power Configurable Adder for Approximate Applications
3.	A Low-Power High-Speed Accuracy-Controllable Approximate Multiplier Design
4.	Optimizing Power-Accuracy trade-off in Approximate Adders
5.	A Simple Yet Efficient Accuracy- Configurable Adder Design
6.	A Low Power CMOS Temperature Sensor Frontend for RFID Tags
7.	Low-Power Addition With Borrow-Save Adders Under Threshold Voltage Variability
8.	A Low-Power Yet High-Speed Configurable Adder for Approximate Computing
9.	Design and Evaluation of Approximate Logarithmic Multipliers for Low Power Error-Tolerant Applications
10.	Improving Error Correction Codes for Multiple-Cell Upsets in Space Applications
11.	A Double Error Correction Code for 32-bit Data Words with Efficient Decoding
12.	An Efficient VLSI Architecture for Convolution Based DWT Using MAC
13.	High Speed Power Efficient Carry Select Adder Design
14.	Design of Majority Logic (ML) Based Approximate Full Adders
15.	High Performance VLSI Architecture for Transpose Form FIR Filter using Integrated Module
16.	Fault-tolerant design and analysis of QCA based circuits

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17.	Unbiased Rounding for HUB Floating-point Addition
18.	Scalable Construction of Approximate Multipliers With Formally Guaranteed Worst Case Error
19.	Combined Pseudo-Exhaustive and Deterministic Testing of Array Multipliers
20.	Nonlinear Binary Codes and Their Utilization for Test
21.	A High-performance and Area-efficient VLSI Architecture for the PRESENT Lightweight Cipher
22.	A Novel approach for design of Real Time Traffic Control System using Verilog HDL
23.	An efficient way of implementing high speed 4-Bit advanced multipliers in FPGA
24.	An Inter-Layer Interconnect BIST Solution for Monolithic 3D ICs
25.	Approximate Reverse Carry Propagate Adder for Energy-Efficient DSP Applications
26.	Built-in Test for Hidden Delay Faults
27.	Design and Verilog HDL Implementation of Carry Skip Adder Using Kogge-Stone Tree Logic
28.	High Speed Efficient Multiplier Design using Reversible Gates
29.	High-Performance NTT Architecture for Large Integer Multiplication
30.	Inexact Arithmetic Circuits for Energy Efficient loT Sensors Data Processing
31.	A High Performance Scan Flip-Flop Design for Serial and Mixed Mode Scan Test
32.	A Single and Adjacent Error Correction Code for Fast Decoding of Critical Bits
33.	Automotive functional safety assurance by post with sequential observation
34.	Parallel Pseudo-Exhaustive Testing of Array Multipliers with Data-Controlled Segmentation
35.	Logic BIST with Capture-per-Clock Hybrid Test Points

36.	Flexible Architecture of Memory BISTs
37.	Efficient Implementations of 4-Bit Burst Error Correction for Memories
38.	Towards Efficient Modular Adders based on Reversible Circuits
39.	Systematic Design of an Approximate Adder: The Optimized Lower Part Constant-OR Adder
40.	Design, Implementation and Verification of 32-Bit ALU with VIO
41.	All Optical Design of Hybrid Adder Circuit Using Terahertz Optical Asymmetric Demultiplexer
42.	A Novel Reversible Synthesis of Array Multiplier
43.	Area and Power Efficient VLSI Architecture of Distributed Arithmetic Based LMS Adaptive Filter
44.	FIR filter design based on FPGA
45.	An Approach to LUT Based Multiplier for Short Word Length DSP Systems
46.	FPGA Implementation of an Improved Watchdog Timer for Safety-critical Applications
47.	Chip Design for Turbo Encoder Module for In-Vehicle System
48.	BINARY TO GRAY CODE CONVERTER IMPLEMENTATION USING QCA
49.	A Novel Design of Flip-Flop Circuits using Quantum Dot Cellular Automata (QCA)
50.	Application of Bit-Serial Arithmetic Units for FPGA Implementation of Convolutional Neural Networks
51.	Design and simulation of CRC encoder and decoder using VHDL/verilog
52.	Time to Digital Converter Based on a Ring Oscillator with Even Number of Non-Inverting Elements
53.	A Channel-Sharable Built-In Self-Test Scheme for Multi-Channel DRAMs
54.	Random Number Generation with LFSR Based Stream Cipher Algorithms
55.	Characterization of Clock Buffers for On-Chip Inter-Circuit Communication in Xilinx FPGAs

56.	Design and Implementation of the Algorithm for RB Multiplication to Derive High-Throughput Digit-Serial Multipliers
57.	FPGA Realization of Speech Encryption Based on Modified Chaotic Logistic Map
58.	VLSI Implementation of Channel Estimation for Millimeter Wave Beam forming Training
59.	Heuristic based Majority/Minority Logic Synthesis for Emerging Technologies
60.	A Low Error Energy-Efficient Fixed-Width Booth Multiplier with Sign-Digit-Based Conditional Probability Estimation
61.	Energy-Efficient Approximate Multiplier Design using Bit Significance-Driven Logic Compression
62.	A Parallel, Energy Efficient Hardware Architecture for the merAligner on FPGA using Chisel HCL
63.	Area and Performance Evaluation of Central DMA Controller in Xilinx Embedded FPGA Designs
64.	Design of Low Power Multiplierless Linear-Phase FIR Filters
65.	Algorithm for Constructing Minimal Representations of Multiple-output Boolean Functions in The Reversible Logic Circuits
66.	FPGA Implementation of Matrix-Vector Multiplication Using Xilinx System Generator
67.	Design and Implementation of Arithmetic and Logic Unit (ALU) using Novel Reversible Gates in Quantum Cellular Automata
68.	Design of Power and Area Efficient Approximate Multipliers
69.	Low-Power Approximate MAC Unit
70.	Efficient Design-for-Test Approach for Networks-on-Chip
71.	Integrating BIST techniques for on-line SoC testing
72.	A Reliable Strong PUF Based on Switched-Capacitor Circuit

73.	Reducing the Hardware Complexity of a Parallel Prefix Adder
74.	Research and implementation of hardware algorithms for multiplying binary numbers
75.	Division circuits using reversible logic gates
	Backend
1.	Low Power 1-Bit Full Adder Using Full-Swing Gate Diffusion Input Technique
2.	Low-Power and Fast Full Adder by Exploring New XOR and XNOR Gates
3.	Low Power 4×4 Bit Multiplier Design using Dadda Algorithm and Optimized Full Adder
4.	Positive Feedback Symmetric Adiabatic Logic against Differential Power Attack
5.	Soft-Error Tolerant Design in Near-Threshold-Voltage Computing
6.	Stateful Memristor-Based Search Architecture
7.	CMOS circuit techniques for Mm –wave communications
8.	Approximate Fully Connected Neural Network Generation
9.	Low Power 4-Bit Arithmetic Logic Unit Using Full-Swing GDI Technique
10.	FPAP: A Folded Architecture for Efficient Computing of Convolutional Neural Networks
11.	Analysis of Optimization Techniques for Low Power VLSI Design
12.	Low Power GDI ALU Design with Mixed Logic Adder Functionality
13.	Design of Reversible Full subtractor using new Reversible EVNL gate for Low Power Applications
14.	Low Leakage Fully Half-Select-Free Robust SRAM Cells with BTI Reliability Analysis
15.	Fractional-Order Differentiators and Integrators with Reduced Circuit Complexity

16.	High speed and low power preset-able modified TSPC D flip-flop design and performance comparison with TSPC D flip-flop
17.	A Low-Power High-Speed Comparator for Precise Applications
18.	High-Density SOT-MRAM Based on Shared Bitline Structure
19.	Two-Phase Read Strategy for Low Energy Variation-Tolerant STT-RAM
20.	Enabling Fast Process Variation and Fault Simulation Through Macromodelling of Analog Components
21.	A SEU/MBU Tolerant SRAM Bit Cell Based on Multi-Input Gate
22.	Design of low power magnitude comparator
23.	Design of Reversible Full subtractor using new Reversible EVNL gate for Low Power Applications
24.	High-performance engineered gate transistor-based compact digital circuits
25.	Sense-Amplifier-Based Flip-Flop With Transition Completion Detection for Low-Voltage Operation