takeoffedu GROUP
(A Division of Youngminds technology Solutions Pvt.Ltd)

CERTIFIED ISO 9001:2015 COMPANY

takeoffedu GROUP

OUR CULTURE | OUR COMMITMENT

(A Division of Youngminds technology Solutions (P).Ltd)

TAKEOFF PROJECTS

Embedded Projects
VLSI Projects
EEE Parojects
MATLAB Projects
PHP Projects
School Projects
Ph.d Assistance New

Java Projects
.Net Projects
NS2 Projects
Android Projects
Paper Publishing New
International Journals New
UGC Approved Journals New
Scopus Indexed Journals New

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2018-2019 M.TECH VLSI IEEE TITLES

S.No	TITLES	DOMAIN
	CORE VLSI	
1	Approximate Quaternary Addition with the Fast Carry Chains of FPGAs	CORE VLSI
2	A Low-Power Configurable Adder for Approximate Applications	CORE VLSI
3	A Low-Power High-Speed Accuracy-Controllable Approximate Multiplier Design	CORE VLSI
4	A Low-Power Yet High-Speed Configurable Adder for Approximate Computing	CORE VLSI
5	A Simple Yet Efficient Accuracy- Configurable Adder Design	CORE VLSI
6	Adaptive Approximation in Arithmetic Circuits: A Low-Power Unsigned Divider Design	CORE VLSI
7	Approximate Hybrid High Radix Encoding for Energy-Efficient Inexact Multipliers	CORE VLSI
8	A Cost-Effective Self-Healing Approach for Reliable Hardware Systems	CORE VLSI
9	Approximate Sum-of-Products Designs Based on Distributed Arithmetic	CORE VLSI
10	Design and Evaluation of Approximate Logarithmic Multipliers for Low Power Error-Tolerant Applications	CORE VLSI
11	Design, Evaluation and Application of Approximate High-Radix Dividers	CORE VLSI
12	Efficient Fixed/Floating-Point Merged Mixed-Precision Multiply-Accumulate Unit for Deep Learning Processors	CORE VLSI
13	Enhancing Fundamental Energy Limits of Field-Coupled Nano computing Circuits	CORE VLSI
14	Exploration of Approximate Multipliers Design Space using Carry Propagation Free Compressors	CORE VLSI
15	Inexact Arithmetic Circuits for Energy Efficient IOT Sensors Data Processing	CORE VLSI
16	Low-Power Addition With Borrow-Save Adders Under Threshold Voltage Variability	CORE VLSI
17	Novel High speed Vedic Multiplier proposal incorporating Adder based on Quaternary Signed Digit number system	CORE VLSI
18	On the Difficulty of Inserting Trojans in Reversible Computing Architectures	CORE VLSI
19	Optimizing Power-Accuracy trade-off in Approximate Adders	CORE VLSI
20	Power Efficient Approximate Booth Multiplier	CORE VLSI
21	Reducing the Hardware Complexity of a Parallel Prefix Adder	CORE VLSI

22	Systematic Design of an Approximate Adder: The Optimized Lower Part Constant-OR Adder	CORE VLSI
23	Towards Efficient Modular Adders based on Reversible Circuits	CORE VLSI
24	A 32-bit 4×4 Bit-Slice RSFQ Matrix Multiplier	CORE VLSI
25	Research and implementation of hardware algorithms for multiplying binary numbers	CORE VLSI
26	Efficient Design for Fixed-Width Adder-Tree	CORE VLSI
27	Architecture Generator for Type-3 Unum Posit Adder/Subtractor	CORE VLSI
	COMMUNICATION	
1	Improving Error Correction Codes for Multiple-Cell Upsets in Space Applications	COMMUNICATION
2	A Single and Adjacent Error Correction Code for fast Decoding of Critical Bits	COMMUNICATION
3	Efficient Implementations of 4-Bit Burst Error Correction for Memories	COMMUNICATION
4	Extending 3-bit Burst Error-Correction Codes With Quadruple Adjacent Error Correction	COMMUNICATION
5	Double Error Cellular Automata-Based Error Correction with Skip-mode Compact Syndrome Coding for Resilient PUF Design	COMMUNICATION
6	A Double Error Correction Code for 32-bit Data Words with Efficient Decoding	COMMUNICATION
7	Basic-Set Trellis Min–Max Decoder Architecture for Non binary LDPC Codes With High-Order Galois Fields	COMMUNICATION
8	An Efficient VLSI Architecture for Convolution Based DWT Using MAC	COMMUNICATION
9	Low-Power Noise-Immune Nano scale Circuit Design Using Coding-Based Partial MRF Method	COMMUNICATION
10	Reconfigurable Decoder for LDPC and Polar Codes	COMMUNICATION
11	Efficient Protection of the Register File in Soft-processors Implemented on Xilinx FPGAs	COMMUNICATION
12	Design and simulation of CRC encoder and decoder using VHDL	COMMUNICATION
	DIGITAL SIGNAL PROCESSING	
1	An Efficient FPGA Implementation of HEVC Intra Prediction	DIGITAL SIGNAL PROCESSING
2	An Area Efficient 1024-Point Low Power Radix-22 FFT Processor With Feed-Forward Multiple Delay Commutators	DIGITAL SIGNAL PROCESSING
3	Low Power Area-Efficient DCT Implementation Based on Markov Random Field-Stochastic Logic	DIGITAL SIGNAL PROCESSING

4	VLSI design of low-cost and high-precision fixed-point reconfigurable FFT processors	DIGITAL SIGNAL PROCESSING
	TESTING	
1	A High Performance Scan Flip-Flop Design for Serial and Mixed Mode Scan Test	TESTING
2	Automotive Functional Safety Assurance by post with Sequential Observation	TESTING
3	Flexible Architecture of Memory BISTs	TESTING
4	Logic BIST with Capture-per-Clock Hybrid Test Points	TESTING
5	Parallel Pseudo-Exhaustive Testing of Array Multipliers with Data-Controlled Segmentation	TESTING
	LOW POWER	
1	Vector Processing-Aware Advanced Clock-Gating Techniques for Low-Power Fused Multiply-Add	LOW POWER
2	Low-Power Approximate Multipliers Using Encoded Partial Products and Approximate Compressors	LOW POWER
3	Toward Energy-Efficient Stochastic Circuits Using Parallel Sobol Sequences	LOW POWER
	BACK END	
1	Low Power 4-Bit Arithmetic Logic Unit Using Full-Swing GDI Technique	BACK END
2	Design of Area-Efficient and Highly Reliable RHBD 10T Memory Cell for Aerospace Applications	BACK END
3	Design Considerations for Energy-Efficient and Variation-Tolerant Nonvolatile Logic	BACK END
4	Effect of Switched-Capacitor CMFB on the Gain of Fully Differential Op-Amp for Design of Integrators	BACK END
5	Passive Noise Shaping in SAR ADC With Improved Efficiency	BACK END
6	A Low-Power Forward and Reverse Body Bias Generator in CMOS 40 nm	BACK END
7	Low Power 1-Bit Full Adder Using Full-Swing Gate Diffusion Input Technique	BACK END
8	Low Power 4×4 Bit Multiplier Design using Dadda Algorithm and Optimized Full Adder	BACK END
9	Low-Power and Fast Full Adder by Exploring New XOR and XNOR Gates	BACK END
10	Sense-Amplifier-Based Flip-Flop With Transition Completion Detection for Low-Voltage Operation	BACK END
11	A 16-mW 1-GS/s With 49.6-dB SNDR TI-SAR ADC for Software-Defined Radio in 65-nm CMOS	BACK END

12	A Droop Measurement Built-in Self-Test Circuit for Digital Low-Dropout Regulators	BACK END
13	A Highly Efficient Composite Class-AB–AB Miller Op-Amp With High Gain and Stable From 15 pF Up To Very Large Capacitive Loads	BACK END
	QCA TECHNOLOGY	
1	A Novel Design of Flip-Flop Circuits using Quantum Dot Cellular Automata (QCA)	QCA TECHNOLOGY
2	A Novel Five-input Multiple-function QCA Threshold Gate	QCA TECHNOLOGY
3	An Energy-aware Model for the Logic Synthesis of Quantum-Dot Cellular Automata	QCA TECHNOLOGY
4	An Exact Method for Design Exploration of Quantum-dot Cellular Automata	QCA TECHNOLOGY
5	Design of Majority Logic (ML) Based Approximate Full Adders	QCA TECHNOLOGY
6	Placement and Routing by Overlapping and Merging QCA Gates	QCA TECHNOLOGY

PROJECT SUPPORTS FOR STUDENTS:

- PROJECT ABSTRACT
- PROJECT IEEE BASE PAPER/ REFERENCE PAPER
- PROJECT PRESENTATION IN PPT FORMAT
- PROJECT REVIEW ASSISTANCE FOR VIVA
- PROJECT DIAGRAMS
- PROJECT SOURCE CODE
- PROJECT REPORT
- PROJECT SCREEN SHOTS
- PROJECT DEMO
- PROJECT EXPLANATION
- PLAGARISM DOCUMENTATION
- INTERNATIONAL JOURNAL/CONFERENCE PUBLISHING
- PROJECT ACCEPTANCE LETTER
- PROJECT COMPLETION CERTIFICATE

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