takeoffedu GROUP
(A Division of Youngmind technology Solutions (P).Ltd)

2017 – 2018 M.TECH VLSI IEEE TITLES

S.NO	TITLES	DOMAIN
1	A Low Error Energy-Efficient Fixed-Width Booth Multiplier with Sign-Digit-Based Conditional Probability Estimation	CORE VLSI
2	A Slack-based Approach to Efficiently Deploy Radix 8 Booth Multipliers	CORE VLSI
3	Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers	CORE VLSI
4	Design of Power and Area Efficient Approximate Multipliers	CORE VLSI
5	Design of Approximate Radix-4 Booth Multipliers for Error-Tolerant Computing	CORE VLSI
6	Design And Synthesis Of Combinational Circuits Using Reversible Decoder In Xilinx	CORE VLSI
7	Majority Logic Formulations for Parallel Adder Designs at Reduced Delay and Circuit Complexity	CORE VLSI
8	A Residue-to-Binary Converter for the Extended Four-Moduli Set $\{2^n - 1, 2^n + 1, 2^{2n} + 1, 2^{2n+p}\}$	CORE VLSI
9	Fast Energy Efficient Radix-16 Sequential Multiplier	CORE VLSI
10	DSP48E Efficient Floating Point Multiplier Architectures on FPGA	CORE VLSI
11	Energy-Efficient VLSI Realization of Binary64 Division With Redundant Number Systems	CORE VLSI
12	Majority-Logic-Optimized Parallel Prefix Carry Look-Ahead Adder Families Using Adiabatic Quantum-Flux-Parametron Logic	CORE VLSI
13	Sign-Magnitude Encoding for Efficient VLSI Realization of Decimal Multiplication	CORE VLSI
14	Design and Analysis of Multiplier Using Approximate 15-4 Compressor	CORE VLSI

www.takeoffprojects.com

15	Energy-Efficient Approximate Multiplier Design using Bit Significance-Driven Logic Compression	CORE VLSI
16	High Performance Parallel Decimal Multipliers using Hybrid BCD Codes	CORE VLSI
17	High-Speed and Low-Power VLSI-Architecture for Inexact Speculative Adder	CORE VLSI
18	Improved 64-bit Radix-16 Booth Multiplier Based on Partial Product Array Height Reduction	CORE VLSI
19	Multi-operand logarithmic addition/subtraction based on Fractional Normalization	CORE VLSI
20	On the Implementation of Computation-in-Memory Parallel Adder	CORE VLSI
21	Optimal Design of Reversible Parity Preserving New Full Adder / Full Subtractor	CORE VLSI
22	Probabilistic Error Analysis of Approximate Recursive Multipliers	CORE VLSI
23	RAP-CLA: A Reconfigurable Approximate Carry Look-Ahead Adder	CORE VLSI
24	RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing	CORE VLSI
25	Comparative study of 16-order FIR filter design using different multiplication techniques	CORE VLSI
26	Low Latency and Low Error Floating-Point Sine/Cosine Function Based TCORDIC Algorithm	CORE VLSI
27	An Optimised 3x3 Shift and Add Multiplier on FPGA	CORE VLSI
28	Optimization of Constant Matrix Multiplication with Low Power and High Throughput	CORE VLSI
29	Realization of a hardware generator for the Sum of Absolute Difference component	CORE VLSI
30	A Structured Visual approach to GALS Modelling and Verification of Communication Circuits	CORE VLSI
31	Low-Latency, Low-Area, and Scalable Systolic-Like Modular Multipliers for *GF(2m)* Based on Irreducible All-One Polynomials	CORE VLSI

www.takeoffprojects.com

32	A Novel Data Format for Approximate Arithmetic Computing	CORE VLSI
33	Automatic Generation of Farmally Prover temper resistant Galioes field multiplier based on generalized masking scheme	CORE VLSI
34	Area-Efficient Architecture for Dual-Mode Double Precision Floating Point Division	CORE VLSI
35	High-Speed and Low-Latency ECC Processor Implementation Over GF(2*m)* on FPGA	CORE VLSI
36	DLAU: A Scalable Deep Learning Accelerator Unit on FPGA	CORE VLSI
37	Low-Complexity Digit-Serial Multiplier Over *GF(2m)* Based on Efficient Toeplitz Block Toeplitz Matrix–Vector Product Decomposition	CORE VLSI
38	Reconfigurable Constant Multiplication for FPGAs	CORE VLSI
39	Hybrid Hardware/Software Floating-Point Implementations for Optimized Area and Throughput Tradeoffs	CORE VLSI
40	Area-time Efficient Architecture of FFT-based Montgomery Multiplication	CORE VLSI
41	Efficient RNS Scalers for the Extended Three-Moduli Set $(2^n -1; 2^{n+p}; 2^n + 1)$	CORE VLSI
42	Digit-Level Serial-In Parallel-Out Multiplier Using Redundant Representation for a Class of Finite Fields	COMMUNICATION
43	Efficient Designs of Multi ported Memory on FPGA	COMMUNICATION
44	Overloaded CDMA Crossbar for Network-On-Chip	COMMUNICATION
45	A Scalable Network-on-Chip Microprocessor With 2.5D Integrated Memory and Accelerator	COMMUNICATION
46	A Custom Accelerator for Homomorphic Encryption Applications	COMMUNICATION
47	A novel method of decoding the BCH code based on norm syndrome to improve the error correction efficiency	COMMUNICATION

www.takeoffprojects.com

48	An Efficient O(*N*) Comparison-Free Sorting Algorithm	COMMUNICATION
49	Efficient Soft Cancelation Decoder Architectures for Polar Codes	COMMUNICATION
50	Fault Space Transformation: A Generic Approach to Counter Differential Fault Analysis and Differential Fault Intensity Analysis on AES-like Block Ciphers	COMMUNICATION
51	Pushing the Limits of Voltage Over-Scaling for Error-Resilient Applications	COMMUNICATION
52	Low Redundancy Matrix-Based codes for Adjacent Error Correction with Parity Sharing	COMMUNICATION
53	Near-Threshold RISC-VCore With DSP Extensions for Scalable IoT Endpoint Devices	COMMUNICATION
54	Efficient Hardware Implementation of Probabilistic Gradient Descent Bit-Flipping	COMMUNICATION
55	Probabilistic Error Modeling for Approximate Adders	COMMUNICATION
56	Novel Solutions of Delta-Sigma Based Rectifying Encoder	COMMUNICATION
57	SPARX - A Side-Channel Protected Processor for ARX-based Cryptography	COMMUNICATION
58	LLR-based Successive-Cancellation List Decoder for Polar Codes with Multi-bit Decision	COMMUNICATION
59	Towards Low Power Approximate DCT Architecture for HEVC Standard	COMMUNICATION
60	High-Throughput and Energy-Efficient Belief Propagation Polar Code Decoder	COMMUNICATION
61	Two Approximate Voting Schemes for Reliable Computing	COMMUNICATION
62	On the VLSI Energy Complexity of LDPC Decoder Circuits	COMMUNICATION
63	Two-Extra-Column Trellis Min–Max Decoder Architecture for Nonbinary LDPC Codes	COMMUNICATION
64	Key Reconciliation Protocols for Error Correction of Silicon PUF Responses	COMMUNICATION
65	A Memory-Based FFT Processor Design With Generalized Efficient Conflict-Free Address Schemes	DIGITAL SIGNAL PROCESSING

www.takeoffprojects.com

66	Algorithm and Architecture Design of Adaptive Filters With Error Nonlinearities	DIGITAL SIGNAL PROCESSING
67	Design and Applications of Approximate Circuits by Gate-Level Pruning	DIGITAL SIGNAL PROCESSING
68	A 4096-Point Radix-4 Memory-Based FFT Using DSP Slices	DIGITAL SIGNAL PROCESSING
69	Hardware efficient multiplier-less multi-level 2D DWT architecture without off-chip RAM	DIGITAL SIGNAL PROCESSING
70	High Performance Integer DCT Architectures for HEVC	DIGITAL SIGNAL PROCESSING
71	Low Complexity and Critical Path based VLSI Architecture for LMS Adaptive Filter using Distributed Arithmetic	DIGITAL SIGNAL PROCESSING
72	Multipliers-Driven Perturbation of Coefficients for Low-Power Operation in Reconfigurable FIR Filters	DIGITAL SIGNAL PROCESSING
73	A Bit plane Decomposition Matrix Based VLSI Integer Transform Architecture for HEVC	DIGITAL SIGNAL PROCESSING
74	Design of Efficient Multiplier less Modified Cosine-Based Comb Decimation Filters: Analysis and Implementation	DIGITAL SIGNAL PROCESSING
75	Software Implementation of the Recursive Discrete Fourier Transform	DIGITAL SIGNAL PROCESSING
76	COMEDI: Combinatorial Election of Diagnostic Vectors From Detection Test Sets for Logic Circuits	TESTING
77	Low-Power Scan-Based Built-In Self-Test Based on Weighted Pseudorandom Test Pattern Generation and Reseeding	TESTING
78	Scalable Approach for Power Droop Reduction During Scan-Based Logic BIST	TESTING
79	Hardware-Efficient Built-In Redundancy Analysis for Memory With Various Spares	TESTING
80	High-Speed Parallel LFSR Architectures Based on Improved State-Space Transformations	TESTING
81	An Improved DCM-based Tunable True Random Number Generator for Xilinx FPGA	TESTING
82	LFSR-Based Generation of Multi cycle Tests	TESTING

www.takeoffprojects.com

83	Low-Power Design for a Digit-Serial Polynomial Basis Finite Field Multiplier Using Factoring Technique	LOW POWER
84	Scenario-Aware Dynamic Power Reduction Using Bias Addition	LOW POWER
85	Hardware/Software Approach to Designing Low-Power RNS-Enhanced Arithmetic Units	LOW POWER
86	Clock-gating of streaming applications for energy efficient implementations on FPGAs	LOW POWER
87	28-nm Latch-Type Sense Amplifier Modification for Coupling Suppression	BACK END
88	A Compact memristor-CMOS hybrid Look-up-table Design and Potential Application in FPGA	BACK END
89	CMCS: Current-Mode Clock Synthesis	BACK END
90	Binary Adder Circuit Design Using Emerging MIGFET Devices	BACK END
91	A 1.8V CMOS Chopper Four-Quadrant Analog Multiplier	BACK END
92	A High-Speed and Power-Efficient Voltage Level Shifter for Dual-Supply Applications	BACK END
93	Delay Analysis for Current Mode Threshold Logic Gate Designs	BACK END
94	A Mapping Methodology of Boolean Logic Circuits on Memristor Crossbar	BACK END
95	A Synthesis Methodology for Ternary Logic Circuits in Emerging Device Technologies	BACK END
96	A Memristor Based Binary Multiplier	BACK END
97	Area and Energy-Efficient Complementary Dual-Modular Redundancy Dynamic Memory for Space Applications	BACK END
98	Bias-Induced Healing of *V*min Failures in Advanced SRAM Arrays	BACK END
99	Design and Low Power Magnitude Comparator	BACK END
100	Design of Low Power, High Performance 2-4 and 4-16 Mixed-Logic Line Decoders	BACK END

www.takeoffprojects.com

101	Energy-Efficient TCAM Search Engine Design Using Priority-Decision in Memory Technology	BACK END
102	High Performance Ternary Adder using CNTFET	BACK END
103	High-performance engineered gate transistor-based compact digital circuits	BACK END
104	Design of Defect and Fault-Tolerant Nonvolatile Spintronic Flip-Flops	BACK END
105	Exploiting Transistor-Level Reconfiguration to Optimize Combinational circuits	BACK END
106	Optimized Memristor-Based Multipliers	BACK END
107	Probability-Driven Multibit Flip-Flop Integration With Clock Gating	BACK END
108	Register – Less NULL Conventional Logic	BACK END
109	Sense Amplifier Half-Buffer (SAHB): A Low-Power High-Performance Asynchronous Logic QDI Cell Template	BACK END
110	Ultra-Low Power, Highly Reliable, and Nonvolatile Hybrid MTJ/CMOS Based Full-Adder for Future VLSI Design	BACK END
111	10T SRAM Using Half-VDD Precharge and Row-Wise Dynamically Powered Read Port for Low Switching Power and Ultralow RBL Leakage	BACK END
112	Fault Tolerant Logic Cell FPGA	BACK END
113	Decimal Full Adders Specially Designed for Quantum-Dot Cellular Automata	QCA TECHNOLOGY
114	Majority Logic Circuits Optimisation by Node Merging	QCA TECHNOLOGY
115	Optimal synthesis of QCA logic circuit eliminating wire-crossings	QCA TECHNOLOGY
116	Heuristic based Majority/Minority Logic Synthesis for Emerging Technologies	QCA TECHNOLOGY
117	Design of non-restoring divider in quantum dot cellular automata technology	QCA TECHNOLOGY

www.takeoffprojects.com

118	NANOcom: A Mosaic Approach For Nano electronic Circuits Design	QCA TECHNOLOGY
119	Reversible logic-based image steganography using quantum dot cellular automata for secure nano communication	QCA TECHNOLOGY
120	Design of Generalized Pipeline Cellular Array in Quantum-Dot Cellular Automata	QCA TECHNOLOGY

www.takeoffprojects.com