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GROUP

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(A Division of Youngminds technology Solutions (P).Ltd)

TAKEOFF PROJECTS

Embedded Projects
VLSI Projects
EEE Projects
MATLAB Projects
School Projects

Java Projects
.Net Projects
NS2 Projects
Android Projects
PHP Projects

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2016 – 2017 M.TECH VLSI IEEE TITLES

S.NO	TITLES	DOMAIN
1	A Fixed-Point Squaring Algorithm Using an Implicit Arbitrary Radix Number System	CORE VLSI
2	An Improved Design of a Reversible Fault Tolerant LUT-Based FPGA	CORE VLSI
3	An Improved Signed Digit Representation Approach for Constant Vector Multiplication	CORE VLSI
4	Area-Delay Efficient Digit-Serial Multiplier Based on *k*-Partitioning Scheme Combined With TMVP Block Recombination Approach	CORE VLSI
5	Area-Delay-Power-Aware Adder Placement Method for RNS Reverse Converter Design	CORE VLSI
6	Efficient Implementation of Scan Register Insertion on Integer Arithmetic Cores for FPGAs	CORE VLSI
7	Logic Synthesis in Reversible PLA	CORE VLSI
8	MAC Unit for Reconfigurable Systems Using Multi- Operand Adders with Double Carry-Save Encoding	CORE VLSI
9	Multi Precision Arithmetic Adders	CORE VLSI
10	Weighted Partitioning for Fast Multiplier-less Multiple Constant Convolution Circuit	CORE VLSI
11	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels	CORE VLSI
12	Low complexity and area efficient reconfigurable multimode inter leaver address generator for multi standard radios	CORE VLSI
13	Efficient implementation of bit-parallel fault tolerant polynomial basis multiplication and squaring over GF(2m)	CORE VLSI

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14	Measuring Improvement When Using HUB Formats to Implement Floating-Point Systems Under Round-to-Nearest	CORE VLSI
15	Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic	CORE VLSI
16	A Modified Partial Product Generator for Redundant Binary Multipliers	CORE VLSI
17	Arithmetic algorithms for extended precisionusing floating-point expansions	CORE VLSI
18	Pre-Encoded Multipliers Based on Non-Redundant Radix-4 Signed-Digit Encoding	CORE VLSI
19	Performance/Power Space Exploration for Binary64 Division Units	CORE VLSI
20	On Efficient Retiming of Fixed-Point Circuits	CORE VLSI
21	Hybrid LUT/Multiplexer FPGA Logic Architectures	CORE VLSI
22	VLSI Design for Convolutive BlindSource Separation	CORE VLSI
23	Concept, Design, and Implementation of Reconfigurable CORDIC	CORE VLSI
24	Ultralow-Energy Variation-Aware Design: Adder Architecture Study	CORE VLSI
25	Floating-Point Butterfly Architecture Based on Binary Signed-Digit Representation	CORE VLSI
26	Design and Implementation of Area-Efficient and Low-Power Configurable Booth-Multiplier	CORE VLSI
27	Design and Analysis of Inexact Floating-Point Adders	CORE VLSI
28	Low-Cost High-Performance VLSI Architecture forMontgomery Modular Multiplication	CORE VLSI
29	High speed hybrid double multiplication architectures using	CORE VLSI

	new serial out bit level mastrovito multiplier	
30	Input-Based Dynamic Reconfiguration of Approximate Arithmetic Units for Video Encoding	CORE VLSI
31	A High-Throughput Energy-Efficient Implementation of Successive Cancellation Decoder for Polar Codes Using Combinational Logic	COMMUNICATION
32	A New Fast and Area-Efficient Adder-Based Sign Detector for RNS $\{2^n - 1, 2^n, 2^n + 1\}$	COMMUNICATION
33	An Efficient Decoder Architecture for Non-binary LDPC Codes with Extended Min-Sum Algorithm	COMMUNICATION
34	An Efficient Eligible Error Locator Polynomial Searching Algorithm and Hardware Architecture for One-Pass Chase BCH Codes Decoding	COMMUNICATION
35	An Efficient Implementation of a Fully Combinational Pipelined S-Box on FPGA	COMMUNICATION
36	CWFP: Novel Collective Write back and Fill Policy for Last-Level DRAM Cache	COMMUNICATION
37	High Performance Reconfigurable Viterbi Decoder Design for Multi-Standard Receiver	COMMUNICATION
38	Reducing the Cost of Triple Adjacent Error Correction in Double Error Correction Orthogonal Latin Square Codes	COMMUNICATION
39	A Multimode Area-Efficient SCL Polar Decoder	COMMUNICATION
40	Optimizing the Implementation of SEC–DAEC Codes in FPGAs	COMMUNICATION
41	A Cache-Assisted Scratchpad Memory for Multiple-Bit-Error Correction	COMMUNICATION
42	High-Performance Pipelined Architecture of Elliptic Curve Scalar Multiplication Over GF($2m$)	COMMUNICATION

43	A High Throughput List Decoder Architecturefor Polar Codes	COMMUNICATION
44	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks	COMMUNICATION
45	A New XOR-Free Approach for Implementation ofConvolutional Encoder	COMMUNICATION
46	An Efficient Single and Double-Adjacent Error Correcting Parallel Decoder for the (24,12) Extended Golay Code	COMMUNICATION
47	A New CDMA Encoding/Decoding Method for on-Chip Communication Network	COMMUNICATION
48	High-Performance Deadlock-Free ID Assignment for Advanced Interconnect Protocols	COMMUNICATION
49	Digital Multiplierless Realization of Two-CoupledBiological Hindmarsh–Rose Neuron Model	COMMUNICATION
50	Low-Cost Multiple Bit Upset Correction in SRAM-Based FPGA Configuration Frames	COMMUNICATION
51	A Method to Design Single Error Correction Codes With Fast Decoding for a Subset of Critical Bits	COMMUNICATION
52	Hardware and Energy-Efficient Stochastic LU Decomposition Scheme for MIMO Receivers	COMMUNICATION
53	Memory-Reduced Turbo Decoding ArchitectureUsing NII Metric Compression	COMMUNICATION
54	In-Field Test for Permanent Faults in FIFO Buffers of NoC Routers	COMMUNICATION
55	A Cellular Network Architecture WithPolynomial Weight Functions	COMMUNICATION
56	A Novel Coding Scheme for Secure Communications in Distributed RFID Systems	COMMUNICATION
57	Enhanced Built-In Self-Repair Techniques for Improving Fabrication Yield and Reliability of Embedded Memories	TESTING

58	A Test Selection Procedure for Improving the Accuracy of Defect Diagnosis	TESTING
59	Low-Cost and High-Reduction Approaches for Power Droop During Launch-On-Shift Scan-Based Logic BIST	TESTING
60	Design for Testability of Sleep Convention Logic	TESTING
61	Computing Seeds for LFSR-Based Test Generation From Non test Cubes	TESTING
62	A Normal I/O Order Radix-2 FFT Architecture to Process Twin Data Streams for MIMO	DIGITAL SIGNAL PROCESSING
63	Low-Power Split-Radix FFT Processors Using Radix-2 Butterfly Units	DIGITAL SIGNAL PROCESSING
64	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications	DIGITAL SIGNAL PROCESSING
65	Efficiency Enablers of Lightweight SDR for MIMO Baseband Processing	DIGITAL SIGNAL PROCESSING
66	Hardware Architectural Support for Caching Partitioned Reconfigurations in Reconfigurable Systems	DIGITAL SIGNAL PROCESSING
67	A Mixed-Decimation MDF Architecturefor Radix-2*k* Parallel FFT	DIGITAL SIGNAL PROCESSING
68	A High-Speed FPGA Implementation of an RSD-Based ECC Processor	DIGITAL SIGNAL PROCESSING
69	A Rule-Based Approach for Minimizing Power Dissipation of Digital Circuits	LOW POWER
70	Multiple Constant Multiplication Algorithmfor High-Speed and Low-Power Design	LOW POWER
71	A Low Power Reconfigurable LFSR	LOW POWER
72	Low-Power Parallel Chien Search ArchitectureUsing a Two-Step Approach	LOW POWER

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74	Graph-Based Transistor Network GenerationMethod for Super gate Design	BACK END
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76	A Low Power Trainable Neuromorphic IntegratedCircuit That Is Tolerant to Device Mismatch	BACK END
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78	PNS-FCR: Flexible Charge RecyclingDynamic Circuit Technique forLow-Power Microprocessors	BACK END
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80	One-Cycle Correction of Timing Errors in PipelinesWith Standard Clocked Elements	BACK END
81	A Single-Ended With Dynamic Feedback Control 8T Sub threshold SRAM Cell	BACK END
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83	A Low-Power Incremental Delta–SigmaADC for CMOS Image Sensors	BACK END
84	Dual Use of Power Lines for Design-for-Testability—A CMOS Receiver Design	BACK END
85	A 55-GHz-Bandwidth Track-and-Hold Amplifierin 28-nm Low-Power CMOS	BACK END
86	Low-Power ASK Detector for Low ModulationIndexes and Rail-to-Rail Input Range	BACK END
87	Low-Power Variation-Tolerant Nonvolatile Lookup Table	BACK END

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89	Design of Efficient BCD Adders in Quantum Dot Cellular Automata	QCA TECHNOLOGY
90	Energy dissipation of quantum-dot cellular automata logic gates	QCA TECHNOLOGY
91	Design of area-delay efficient adder based circuits in quantum dot cellular automata	QCA TECHNOLOGY
92	USE: A Universal, Scalable and Efficient clocking scheme for QCA	QCA TECHNOLOGY
93	Coplanar Full Adder in Quantum-Dot Cellular Automata via Clock-Zone Based Crossover	QCA TECHNOLOGY
94	Design and simulation of Turbo encoder in quantum-dot cellular automata	QCA TECHNOLOGY
95	Design and Analysis of Digital Circuits Using QCA Logic	QCA TECHNOLOGY
96	Design and simulation of single layered Logic Generator Block using Quantum Dot Cellular Automata	QCA TECHNOLOGY

PROJECT SUPPORTS FOR STUDENTS:

- PROJECT ABSTRACT
- PROJECT IEEE BASE PAPER/ REFERENCE PAPER
- PROJECT PRESENTATION IN PPT FORMAT
- PROJECT REVIEW ASSISTANCE FOR VIVA
- PROJECT DIAGRAMS
- PROJECT SOURCE CODE
- PROJECT REPORT
- PROJECT SCREEN SHOTS

- PROJECT DEMO
- PROJECT EXPLANATION
- PLAGARISM DOCUMENTATION
- INTERNATIONAL JOURNAL/CONFERENCE PUBLISHING
- PROJECT ACCEPTANCE LETTER
- PROJECT COMPLETION CERTIFICATE

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