A High Performance Scan Flip-Flop Design for Serial and Mixed Mode Scan Test

Abstract:
Over the years, serial scan design has become the defacto Design for Testability (DFT) technique. The ease of testing and high test coverage has made it gain widespread industrial acceptance. However, there are penalties associated with the serial scan design. These penalties include performance degradation, test data volume, test application time, and test power dissipation. The performance overhead of scan design is due to the scan multiplexers added to the inputs of every flip-flop. In today’s very high-speed designs with minimum possible combinational depth, the performance degradation caused by scan multiplexer has become magnified. Hence to maintain circuit performance the timing overhead of scan design must be addressed. In this paper, we propose a new scan flip-flop design that eliminates the performance overhead of serial scan. The proposed design removes the scan multiplexer from the functional path. The proposed design can help in improving the functional frequency of performance critical designs. Furthermore, the proposed design can be used as a common scan flip-flop in “mixed scan” test wherein it can be used as a serial scan cell as well as a Random Access Scan (RAS) cell. The mixed scan test architecture has been implemented using the proposed scan flip-flop. The experimental results show a promising reduction in interconnect wire length, test time, and test data volume, compared to the state-of-the-art random access scan and multiple serial scan implementations. The proposed architecture of this paper analysis the delay and area using Xilinx 14.3.

Existing Method:
Testing of highly complex SoC designs is a big challenge faced by VLSI test community nowadays. Scan design is the only DFT approach that can effectively test a highly complex design with very high fault coverage. The objective of scan design is to achieve full controllability and observability of every flip-flop in the design. In a full scan design, each flip-flop is replaced by a scan flip-flop. A scan flip-flop is nothing but a muxed input master-slave based D type flip-flop. The scan multiplexer has two inputs: data input (D) and scan input (SI). The input selection is performed using a control signal called test enable (TE). In functional mode, data input is selected.
and the scan flip-flop function as a regular flip-flop. In test mode, scan input is selected, and all the scan flip-flops connect in a serial fashion to form one or more serial shift register(s). The serial shift register(s) is popularly known as scan chain(s). All flip-flops of the scan chain are loaded with desired data by consecutive application of the clock signal. A full scan design reduces the sequential test problem to combinational test problem.

**Proposed Method:**
A new scan flip-flop design that can be used as both a serial scan cell as well as a random access Scan cell. The major advantages of the proposed scan flip-flop design are as follows:
1) It eliminates the performance penalty of the serial scan by removing scan multiplexer from the functional path.
2) It can be used both as a serial scan cell as well as a RAS cell, in the mixed mode scan test.
3) The proposed design does not introduce any extra control signal and uses the test control signal as a quasi-sequential or low-frequency scan clock.
4) The new scan flip-flop is capable of applying all the tests that can be applied with a conventional scan flip-flop. The proposed design fully complies with the existing industry design and test flow.

**Applications**
1) Automatic test pattern generation
2) Testing

**Advantages**
1) High speed
2) Area and delay reduced

**System Configuration:**
In the hardware part a normal computer where Xilinx ISE 14.3 software can be easily operated is required, i.e., with a minimum system configuration

**HARDWARE REQUIREMENT**
Processor - Pentium –III

Speed - 1.1 GHz

RAM - 1 GB (min)

Hard Disk - 40 GB

Floppy Drive - 1.44 MB

Key Board - Standard Windows Keyboard

Mouse - Two or Three Button Mouse

Monitor - SVGA

SOFTWARE REQUIREMENTS


❖ Front End : Modelsim 6.3 for Debugging and Xilinx 14.3 for Synthesis and Hard Ware Implementation

❖ This software’s where Verilog source code can be used for design implementation.