Design and simulation of CRC encoder and decoder using VHDL

ABSTRACT

Cyclic Redundancy Check (CRC) technique is an efficient error detection method which used to detect single and burst errors. CRC technique adds redundancy bits to the original data. The redundancy bits represent the remainder of division between the original message and the selected polynomial. At the receiver side, the received data can be recognized as valid or not. In this paper, an efficient CRC (8) encoder and decoder circuits have been designed and implemented using VHDL. Xilinx ISE 14.3 Simulator is used for circuits verification and validation for CRC (Cyclic Redundancy Checking with an input 8-bit polynomial), 5 and 8-bit input data. The results reveal that the proposed circuits are efficient in terms of hardware utilization rate.

EXISTING SYSTEM:

Cyclical Redundancy Check (CRC) is a kind of important linear block code, which has the advantages of easy coding and decoding as well as strong abilities of checking errors and correcting errors. Therefore, it was widely used in the field of communications and industrial measurement and control system whose industrial environment was even worse. The evolving world of telecommunications requires increasing reliability and speed in communications. Reliability in information storage and transmission is provided by coding techniques. Information is usually coded in bit streams and transmitted over the communication medium, channel.

PROPOSED SYSTEM:

The communication media is prone to errors due to noise present in the analog portion of the channel. Therefore errors have to be detected and corrected while decoding. CRC is an error-detecting code designed to detect accidental changes to raw computer data, and is commonly used in digital networks and storage devices such as hard disk drives. Blocks of data entering
these systems get a short check value attached, derived from the remainder of a polynomial division of their contents; on retrieval the calculation is repeated, and corrective action can be taken against presumed data corruption if the check values do not match. The CRC was invented by W. Wesley Peterson in 1961. CRC is an error detecting code that is widely used to detect corruption in blocks of data that have been transmitted or stored.

Applications

1) Communications
2) Digital signal processing

Advantages

More reliable, delay and power reduced

System Configuration:

In the hardware part a normal computer where Xilinx ISE 14.3 software can be easily operated is required, i.e., with a minimum system configuration

HARDWARE REQUIREMENT

Processor - Pentium –III

Speed - 1.1 GHz

RAM - 1 GB (min)

Hard Disk - 40 GB

Floppy Drive - 1.44 MB

Key Board - Standard Windows Keyboard

Mouse - Two or Three Button Mouse
Software Requirements

- Front End: Modelsim 6.3 For Debugging And Xilinx 14.3 For Synthesis And Hard Ware Implementation

*This Software’s where Verilog Source Code Can Be Used For Design Implementation.