Efficient Implementations of 4-Bit Burst Error Correction for Memories

ABSTRACT

In recent years, there has been a growing interest in error correction codes that can correct localized errors in memories. This is due to the larger fraction of radiation induced error events that affect several nearby memory cells as technology scales. Initially, codes that can correct single and double adjacent errors were proposed. More recently, 3-bit burst error correction codes have also been presented. The next step is to provide efficient 4-bit burst error correction for memories. The issue is that as the error correction capability increases so does the overheads required implementing the codes in terms of parity check bits and encoding and decoding complexity. In this paper, efficient solutions to protect memories against 4-bit bursts are presented. The first one is the use of two interleaved single and double adjacent error correction codes while in the second, efficient 4-bit burst error correction codes are presented. The first solution reduces the decoding complexity and delay at the cost of having more parity check bits while the second tries to reduce the decoding complexity when using the minimum number of parity check bits. Both solutions have been evaluated and compared to an interleaved single error correction code and with existing burst error correction codes to better understand the overheads needed to achieve the protection against 4-bit burst errors.

Existing System:

Before discussing the proposed schemes, it is useful to have an overview of the 4-bit burst error correction codes that have been proposed so far to protect memories. Most of those schemes are based on the use of a two dimensional product code or matrix code. In those codes, data bits are arranged in the format of a matrix and parity bits are added horizontally and vertically. Depending on the horizontal and vertical codes used, different error correction capabilities can be achieved.
Proposed System:

Instead of a common binary matrix code, a method to design 5-bit burst error correction codes using a decimal matrix code is presented. Although this method extends the correction ability, it requires a large amount of parity bits. To obtain the same reliability with lower redundancy, a kind of low redundancy matrix-based codes with parity sharing is presented. In this scheme, the extended Hamming codes per row and parity codes per column are combined with the use of the parity sharing technique to reduce the number of parity check bits needed. However, in this code as well as in the previous ones, the number of parity bits is still well above the theoretical minimum. This means that their use implies a significant overhead in terms of memory size. In the following, two solutions to provide 4-bit burst error correction are described. The first one is based on the interleaving of SEC-DAEC codes while in the second optimized 4-bit burst error correction codes are presented.

Applications

1) Communications
2) Digital signal processing

Advantages

Area, delay and power reduced

System Configuration:

In the hardware part a normal computer where Xilinx ISE 14.3 software can be easily operated is required, i.e., with a minimum system configuration.

HARDWARE REQUIREMENT

<table>
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<tr>
<th>Processor</th>
<th>Pentium –III</th>
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<td>Speed</td>
<td>1.1 GHz</td>
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</table>
RAM              -  1 GB (min)

Hard Disk        -  40 GB

Floppy Drive     -  1.44 MB

Key Board        -  Standard Windows Keyboard

Mouse            -  Two or Three Button Mouse

Monitor          -  SVGA

Software Requirements

- Front End: Modelsim 6.3 For Debugging And Xilinx 14.3 For Synthesis And Hard Ware Implementation

*This Software’s where Verilog Source Code Can Be Used For Design Implementation.