Placement and Routing by Overlapping and Merging QCA Gates

Abstract:
The QCA gate-level design introduces new challenges to the traditional mapping, placement, and routing flow. First, the wires consume more than 90% of total area. In addition, even a combinational circuit requires a clock scheme, and all internal paths should be balanced. This work proposes a novel approach to automatically map a gate-level circuit onto a QCA layout by using a merge overlapping approach, and a universal clock scheme to provide scalability. First, the circuit is decomposed into a set of overlapping sub graph partitions. This decomposition is guided by reconvergent paths. For each subgraph, more than one customized QCA layout cell is generated on-the-fly. During the last step, a merge overlapping algorithm rebuilds the entire circuit to produce the final layout. All inter and intra-partition wires should be balanced according to the adopted clock scheme. Our approach reduces the total area in more than 50% in comparison to a previous approach based on standard-cell QCA libraries. Finally, all layouts were validated on QCADesigner simulator to verify the design rules.

Existing work:
Low power operation, energy dissipation, scaling, and reliability are some challenges currently being faced by silicon-based technology. To overcome these challenges at the nanoscale, new approaches have been proposed. Quantum-Dot Cellular Automata (QCA) is a promising alternative to silicon since this technology operates using extremely low power, being able to reach high clock frequencies and nanoscale sizes. Although QCA has been introduced two decades ago, there are still few tools to support a basic design flow such as logic synthesis, placement, and routing. One of the major differences from the silicon-based design flow is the signal synchronism, where even for a combinational QCA circuit, clocking schemes are required. All signals for any gate should arrive at the same time. Most previous approaches are based on handmade and irregular size clock zones, which are not suitable to be included in an automatic technology mapping flow.

Proposed work:
We introduce a new approach to automatically perform the mapping, placement, and routing of QCA circuits. Our solution reduces wiring and total area by using a merge overlapping approach to explore reconvergent paths. Moreover, we propose a heuristic to reduce the solution design space. In addition, different from previous QCA placement and routing proposals, our final layouts have been validated on QCADesigner simulator.

Applications:
- Low power applications
- Quantum computing.

Advantages:
- Delay and Area.

System Configuration:

In the hardware part a normal computer where QCAD software can be easily operated is required, i.e., with a minimum system configuration.

HARDWARE REQUIREMENT

- **Processor**: Pentium –III
- **Speed**: 1.1 GHz
- **RAM**: 1 GB (min)
- **Hard Disk**: 40 GB
- **Floppy Drive**: 1.44 MB
- **Key Board**: Standard Windows Keyboard
- **Mouse**: Two or Three Button Mouse
SOFTWARE REQUIREMENTS

- Tools: QCAD tools