A NOVEL FIVE-INPUT MULTIPLE-FUNCTION QCA THRESHOLD GATE

ABSTRACT:
QCA (Quantum-dot Cellular Automata) is a promising new technology with low power consumption and high speed that allows the design of nanoscale integrated circuits. The 3-input/1-output majority gate is the basic building block in QCA circuits. This work presents a new design of a multi-output, 5-input majority gate. Our proposed gate is quite useful because its outputs can present different configurations with several logical functions at once, enabling the design of smaller circuits. Also, the proposed gate is a feasible solution for the recently proposed USE (Universal, Scalar and Efficient) clocking scheme. In order to demonstrate the flexibility and area efficiency of our 5-input majority gates we implement two designs: a full adder and a RAM cell block. These designs have been implemented using a free and a regular (USE) clock schemes. Our results show area reductions up to 50% compared to state-of-the-art designs.

Existing work:
A QCA cell is basically a nanometric square with four quantum dots and two electrons that can perform tunneling between the dots. Due to Coulomb interactions, there are only two stable configurations of the electrons inside the cell. The black dots are the quantum dots containing an electron. Polarizations $P = -1$ and $P = +1$ represent logic states 0 and 1, respectively. Bistable cells are locally connected through field effect forces and can be organized in such a way that computation is performed. The inverter and the majority voter gates are the basic elements of QCA circuits. These two elements form a universal gate that can be used to implement any logical function. For instance, we can build 2-input AND/OR gates by fixing one of the inputs of a 3-input majority gate. Moreover, we can configure a 5-input majority gate (MAJ5) to perform a series of complex logical functions, which is useful to design area efficient circuits. In sum, we can design more complex circuits using these basic majority gate building blocks.

Proposed work:
A new clocking scheme, namely USE (Universal, Scalable and Efficient), has been proposed for clock distribution in QCA circuits. It solves one of the most limiting factors of existing clock schemes, the implementation of feedback paths, which facilitates QCA circuit routing, and also avoids thermodynamics problems. With this clock scheme one can focus on the design of the circuit and ignore those problems. Also, a standard cell library has been designed based on USE clock scheme. Many MAJ5 designs have been proposed, but none of them is suitable to USE clock scheme. In this work we present a multi-output, 5-input majority gate that takes into account the restrictions that USE scheme brings to the information flow of a QCA circuit. We use the proposed gate to implement two circuits, a full adder and a RAM cell. In addition, we implement two layouts for each circuit, one using USE clock scheme and another without any clock restriction (free clock scheme). We compare, in terms of area and delay, our designs with the state-of-the-art equivalent ones.

Applications:

- Low power applications
- Quantum computing.

Advantages:

- Delay and Area.

System Configuration:

In the hardware part a normal computer where QCAD software can be easily operated is required, i.e., with a minimum system configuration.

HARDWARE REQUIREMENT

- **Processor**: Pentium –III
- **Speed**: 1.1 GHz
- **RAM**: 1 GB (min)
Hard Disk  -  40 GB

Floppy Drive  -  1.44 MB

Key Board  -  Standard Windows Keyboard

Mouse  -  Two or Three Button Mouse

Monitor  -  SVGA

SOFTWARE REQUIREMENTS

- Tools  :  QCAD tools