A Novel Design of Flip-Flop Circuits using Quantum Dot Cellular Automata (QCA)

Abstract:

As the device dimension is shrinking day by day the conventional transistor based CMOS technology encounters serious hindrances due to the physical barriers of the technology such as ultra-thin gate oxides, short channel effects, leakage currents & excessive power dissipation at nano scale regimes. Quantum Dot Cellular Automata is an alternate challenging quantum phenomenon that provides a completely different computational platform to design digital logic circuits using quantum dots confined in the potential well to effectively process and transfer information at nano level as a competitor of traditional CMOS based technology. This paper has demonstrated the implementation of circuits like D, T and JK flip flops using a derived expression from SR flip-flop. The kink energy and energy dissipations has been calculated to determine the robustness of the designed flip-flops. The simulation results have been verified using QCA Designer simulation tool.

Existing work:

Due to the rapid development of technology, the scenario of digital industry has changed in the past few years. Intel cofounder Gordon Moore in 1960 predicted that the number of transistors on a single chip will double in every eighteen months. According to his prediction, the conventional CMOS based devices advanced from micron to submicron, submicron to deep submicron and to nanometer regime over last five decades. But the scaling of CMOS devices at nano scale affects the performance of several factors like heat dissipation and leakage currents. The heat generated can no longer dissipate and results in damage of the chip as more and more devices are packed into the same area.

Proposed work:

Flip-flops are sequential circuits whose output depends both on the present input as well as the past output. It is a one bit binary storage device capable of storing binary information ‘1’ or
In this paper, most commonly used three types flip-flops namely D, T & JK flipflop are designed from the derived equations of SR flip-flop.

In this paper we have developed a standard equation from SR flip flop and using that equation other flip flops like D, T and JK flip-flops are subsequently designed. This is a new approach of designing flip-flops with less hardware complexity in nanotechnology. Any memory storage device can be built using the flip-flops designed in the above mentioned approach. The layout has been generated and simulation results are verified using QCA Designer simulation tool.

**Applications:**
- Low power applications
- Quantum computing.

**Advantages:**
- Delay and Area.

**System Configuration:**

In the hardware part a normal computer where QCAD software can be easily operated is required, i.e., with a minimum system configuration.

**HARDWARE REQUIREMENT**

- **Processor**
  - Pentium –III
- **Speed**
  - 1.1 GHz
- **RAM**
  - 1 GB (min)
- **Hard Disk**
  - 40 GB
- **Floppy Drive**
  - 1.44 MB
- **Key Board**
  - Standard Windows Keyboard
Mouse - Two or Three Button Mouse

Monitor - SVGA

SOFTWARE REQUIREMENTS

- Tools: QCAD tools