LFSR-Based Generation of Multicycle Tests

Abstract:

The multicycle test set whose scan-in states are compressed into seeds for an LFSR, and whose primary input vectors are held constant during the application of a multicycle test. The goal of computing multicycle tests is to provide test compaction that reduces both the test application time and the test data volume. To avoid sequential test generation, the procedure uses a single cycle test set to guide the computation of multicycle tests. The procedure optimizes every multicycle test, and increases the number of faults it detects, by adjusting its seed, primary input vector, and number of functional clock cycles. Optimizing the seed instead of the scan-in state avoids the computation of scan-in states for which seeds do not exist. Experimental results for benchmark circuits are presented to demonstrate the effectiveness of the procedure.

Existing system:

The scan-in and scan-out operations of a test, a single cycle test has a single functional clock cycle, while a multicycle test has one or more functional clock cycles. Multicycle tests were considered. Their effectiveness for test compaction was demonstrated and results from the following observations. During a functional clock cycle of a test, the combinational logic of the circuit receives an input pattern that can be used for detecting faults. A larger number of functional clock cycles allows more faults to be detected. As a result, a multicycle test may detect more faults than a single-cycle test. With more detected faults for every test, the number of tests is reduced.

Proposed system:

The modification of a seed $s_i$ is implemented by complementing bits of $s_i$ one by one, and recomputing the test $t$ that the LFSR produces. A bit complementation is accepted when it satisfies certain objectives (these objectives are related to the generation of diagnostic tests). In the procedure described the bits of $s_i$ and $v_i$, as well as the value of $l_i$, are modified together in order to produce an effective multicycle test. The target faults are single stuck-at faults. The procedure
is developed assuming that an LFSR is given. This is also describes a modified binary search process for selecting an LFSR out of a given set of available LFSRs.

Applications

1) Testing.

Advantages

1) High speed
2) Area and delay reduced

System Configuration:

In the hardware part a normal computer where Xilinx ISE 14.3 software can be easily operated is required, i.e., with a minimum system configuration.

HARDWARE REQUIREMENT

Processor - Pentium III
Speed - 1.1 GHz
RAM - 1 GB (min)
Hard Disk - 40 GB
Floppy Drive - 1.44 MB
Key Board - Standard Windows Keyboard
Mouse - Two or Three Button Mouse
Monitor - SVGA
SOFTWARE REQUIREMENTS


❖ Front End : Modelsim 6.3 for Debugging and Xilinx 14.3 for Synthesis and Hardware Implementation

❖ This software's where Verilog source code can be used for design implementation.