Hardware-Efficient Built-In Redundancy Analysis for Memory with Various Spares

Abstract:
Memory capacity continues to increase, and many semiconductor manufacturing companies are trying to stack memory dice for larger memory capacities. Therefore, built-in redundancy analysis (BIRA) is of utmost importance because the probability of fault occurrence increases with a larger memory capacity. A traditional spare structure that consists of simpler rows and columns is somewhat inadequate for multiple memory blocks BIRA because the hardware overhead and spare allocation efficiency are degraded. The proposed BIRA uses various types of spares and can achieve a higher yield than a simple row and column spare structure. Herein, we propose a BIRA that can achieve an optimal repair rate using various spare types. The proposed analyzer can exhaustively search not only row and column spare types but also global and local spare types. In addition, this paper proposes a fault-storing content-addressable memory (CAM) structure. The proposed CAM is small and collects faults efficiently. The experimental results show a high repair rate with a small hardware overhead and a short analysis time.

Existing system:
As the capacity and density of memory gradually increases in recent times because of consumer demand, technical limitations in analysis time and the capacity of 2-D memory arises. Therefore, 3-D semiconductor devices become important to overcome these technical limitations and it is expected that the demand for 3-D memory will increase in the near future. Further development of diagnosis and repair techniques is required under these circumstances to maximize the revenue of semiconductor companies. This requires built-in self-test (BIST) and built-in redundancy analysis (BIRA). Since a 3-D semiconductor usually has unused space on the base layer, this space can be used to accommodate additional functions such as BIRA and BIST.
Proposed system:
To obtain a higher repair rate, the proposed BIRA uses various spares such as common spares, local spares, and global spares. Using these spares, the proposed BIRA can achieve a normalized repair rate and a higher repair rate than the conventional spare structure. The explanations for the feature of each spare are given later. In a 3-D memory block, there can be a vertical relationship between each block using spare sharing between dice; there can also be a horizontal relationship within the same die. In order to reduce the hardware overhead, a storage structure of the fault collection unit is devised. And an analyzer is developed to exhaustively search every repair case. Although the number of cases required for the exhaustive combinations of the various spares is large, this onerous analysis time can be overcome by simplifying the search.

Applications
1) Built-in redundancy analysis
2) Testing

Advantages
1) High speed
2) Area and delay reduced

System Configuration:
In the hardware part, a normal computer where Xilinx ISE 14.3 software can be easily operated is required, i.e., with a minimum system configuration.

HARDWARE REQUIREMENT

<table>
<thead>
<tr>
<th>Processor</th>
<th>Pentium-III</th>
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<tbody>
<tr>
<td>Speed</td>
<td>1.1 GHz</td>
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SOFTWARE REQUIREMENTS

- RAM: 1 GB (min)
- Hard Disk: 40 GB
- Floppy Drive: 1.44 MB
- Key Board: Standard Windows Keyboard
- Mouse: Two or Three Button Mouse
- Monitor: SVGA

- Front End: ModelSim 6.3 for Debugging and Xilinx 14.3 for Synthesis and Hardware Implementation
- This software’s where Verilog source code can be used for design implementation.