COMEDI Combinatorial Election of Diagnostic Vectors From Detection Test Sets for Logic Circuits

Abstract:

The modern automatic test pattern generation (ATPG) tools can efficiently produce near-optimal test sets with high fault-coverage for a circuit-under-test, a diagnostic testset (DTS), which is needed for fault localization, is much more challenging to construct. The DTS is used to analyze the responses of failing chips during manufacturing test for the purpose of identifying the root cause of observed errors. In this paper, a novel technique for selecting a powerful DTS for stuck at faults from a pool of ATPG detection vectors is proposed. Unlike existing methods, this technique does not use any diagnostic test generation, circuit modification, or miter-based approach. It constructs a combinatorial cover of the pool to determine a test set with high diagnostic coverage (DC). Two variants of the covering algorithm are proposed based on this technique. The experimental results on several combinational and scan-based benchmark circuits demonstrate the effectiveness of our method in terms of the size of the DTS, DC, and CPU time.

Existing system:

ATPG tools employ powerful heuristics and are capable of generating efficient and compact test sets for a circuit-under-test (CUT). These tools provide tests with high fault coverage, and identify redundant faults in the CUT to a large extent, even though the underlying problem is known to be computationally hard. However, the production tests are primarily aimed only for fault detection and they may not be very efficient for diagnosis. Note that a fault is usually detected in more than one output of the CUT for a given test; also, there are several test vectors that can detect the same fault. The ATPG tools aim to minimize the size of the test set and maximize fault coverage. Needless to say, the test sets, thus generated, are not unique and their diagnostic coverage (DC) may also be diverse.

Proposed system:

Our solution is based on the diversity of the test sets that is observed when an ATPG tool is invoked multiple times on a given circuit netlist. Our method is simple and needs only...
an input/output experiment with a pool of detection test sets and a fault simulator. We do not require running diagnostic ATPG or adopting any circuit-modification, SAT-based approaches, or miter-based techniques. The proposed method is purely combinatorial in nature, that of finding a cover of a response-matrix, which is obtained by invoking an ATPG and fault simulation tools multiple times on the CUT netlist. We propose a compact representation of the response matrix so as to reduce computational time and space complexity. We propose two variants of an algorithm, both based on the same framework. Algorithm 1 generates a response matrix for the entire test pool and aims at finding a diagnostic test cover following a greedy approach. Algorithm 2 runs faster as it performs partial simulation of the test pool while determining diagnostic test cover.

**Applications**

1) Automatic test pattern generation
2) Testing

**Advantages**

1) High speed
2) Area and delay reduced

**System Configuration:**

In the hardware part, a normal computer where Xilinx ISE 14.3 software can be easily operated is required, i.e., with a minimum system configuration

**HARDWARE REQUIREMENT**

<table>
<thead>
<tr>
<th>Processor</th>
<th>Pentium –III</th>
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<tbody>
<tr>
<td>Speed</td>
<td>1.1 GHz</td>
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SOFTWARE REQUIREMENTS


- Front End: Modelsim 6.3 for Debugging and Xilinx 14.3 for Synthesis and Hardware Implementation

- This software's where Verilog source code can be used for design implementation.