Algorithm and Architecture Design of Adaptive Filters With Error Nonlinearities

Abstract:

The framework based on the logarithmic number system to implement adaptive filters with error nonlinearities in hardware. The framework is demonstrated through pipelined implementations of two recently proposed adaptive filtering algorithms based on logarithmic cost, namely, least mean logarithmic square (LMLS) and least logarithmic absolute difference (LLAD). To the best of our knowledge, the proposed architectures are the first attempts to implement both LMLS and LLAD algorithms in hardware. We derive error computing algorithms to realize the nonlinear error functions for LMLS and LLAD and map them onto hardware. We also propose a novel variable-\(\alpha\) scheme to enhance the original LMLS algorithm and prove its robustness and suitability for VLSI implementations in practical applications. Detailed bit width and error analysis are carried out for the proposed VLSI fixed point implementations. Post layout implementation results show that with an additional multiplier over conventional least mean square (LMS), improvement in steady-state mean square deviation performance can be achieved and with the proposed variable-\(\alpha\) scheme, the improvement can be achieved without compromising the convergence. We will show that LMLS can potentially replace LMS in practical applications, by demonstrating a proof-of-concept by extending the framework to transform domain adaptive filters.

Existing system:

The least mean square (LMS) algorithm is by far the most popular adaptive algorithm because of its simple structure and robustness. Many variants of LMS addressing different issues of the original algorithm have been suggested and analyzed extensively in the literature. Of particular importance is the class of LMS algorithms with error nonlinearities. The earliest among them is the least mean fourth (LMF) algorithm, whose cost function is error raised to the fourth power instead of the means square error (MSE). Capturing higher order statistics rather than their energy is very much useful when data are non-Gaussian, and hence, LMF is know to perform
better than the LMS algorithm in the case of non-Gaussian noise and in low signal-to-noise ratio (SNR) environments, however, suffers from stability issues. In an attempt to address this problem, a controlled mixture of LMF and LMS algorithms that results in least mean mixed norm is proposed.

**Proposed system:**

The delayed adaptation concept can be extended to LMLS for its efficient VLSI implementation. Fixed point division is quite a bit more complicated than fixed point multiplication, and usually takes a lot more cycles than performing a multiplication. Thus, we use logarithmic number system (LNS), which simplifies these calculations to a great extent. However, addition and subtraction get complicated with LNS and we have addition in the denominator of the LMLS algorithm \((1 + \alpha e^2(n))\). Moreover, logarithmic and antilogarithmic conversions incur errors, which can adversely affect the convergence of the adaptive algorithms.

**Applications**

1) Fast fourier transforms
2) Digital signal processing

**Advantages**

1) High speed.
2) Area and delay reduced

**System Configuration:**

In the hardware part a normal computer where Xilinx ISE 14.3 software can be easily operated is required, i.e., with a minimum system configuration

**HARDWARE REQUIREMENT**
Processor - Pentium –III

Speed - 1.1 GHz

RAM - 1 GB (min)

Hard Disk - 40 GB

Floppy Drive - 1.44 MB

Key Board - Standard Windows Keyboard

Mouse - Two or Three Button Mouse

Monitor - SVGA

SOFTWARE REQUIREMENTS


❖ Front End : Modelsim 6.3 for Debugging and Xilinx 14.3 for Synthesis and Hard Ware Implementation

❖ This software’s where Verilog source code can be used for design implementation.