Towards Low Power Approximate DCT Architecture for HEVC Standard

Abstract:

Video processing performed directly on IoT nodes is one of the most performance as well as energy demanding applications for current IoT technology. In order to support real-time high-definition video, energy-reduction optimizations have to be introduced at all levels of the video processing chain. This paper deals with an efficient implementation of Discrete Cosine Transform (DCT) blocks employed in video compression based on the High Efficiency Video Coding (HEVC) standard. The proposed multiplierless 4-input DCT implementations contain approximate adders and subtractors that were obtained using genetic programming. In order to manage the complexity of evolutionary approximation and provide formal guarantees in terms of errors of key circuit components, the worst and average errors were determined exactly by means of Binary decision diagrams. Under conditions of our experiments, approximate 4-input DCTs show better quality/power trade-offs than relevant implementations available in the literature. Power reduction for the same error was obtained in comparison with a recent highly optimized implementation.

Existing system

Small embedded systems connected to Internet of Things (IoT) are expected to be a new infrastructure of the information society. These systems range from simple smart sensors to advanced embedded applications requiring considerable computing resources. In order to support real-time coding and decoding of high definition video on low cost devices, energy consumption optimization has to be introduced at all levels of the video processing system. One of the most frequently performed and thus energy-demanding operations is the Discrete Cosine Transform (DCT) block. In commonly optimized DCT blocks, bit width of all operations is reduced as much as possible, multipliers are replaced with additions, subtractions and shifts, and less important logic is pruned in order to reduce power consumption.
Proposed system

This deals with a deep optimization and approximation of the DCT block employed in the state of the art High Efficiency Video Coding (HEVC) standard. In addition to the common optimization techniques, we propose to approximate adders and subtractors of a multiplierless DCT in such a way that the resulting error is kept under a predefined threshold. As the error of addition/subtraction is computed formally, without applying circuit simulation, it is always guaranteed that the target error is never exceeded. The error calculation procedure is based on relaxed equivalence checking using Binary Decision Diagrams (BDDs). BDDs are also used to analyze power consumption during the approximation process.

Applications

1) Communications  
2) Digital signal processing

Advantages

Area, delay and power reduced

System Configuration:-

In the hardware part a normal computer where Xilinx ISE 14.3 software can be easily operated is required, i.e., with a minimum system configuration

HARDWARE REQUIREMENT

<table>
<thead>
<tr>
<th>Processor</th>
<th>Pentium –III</th>
</tr>
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<tbody>
<tr>
<td>Speed</td>
<td>1.1 GHz</td>
</tr>
<tr>
<td>RAM</td>
<td>1 GB (min)</td>
</tr>
<tr>
<td>Hard Disk</td>
<td>40 GB</td>
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</tbody>
</table>
SOFTWARE REQUIREMENTS


❖ Front End : Modelsim 6.3 for Debugging and Xilinx 14.3 for Synthesis and Hardware Implementation

This software’s where Verilog source code can be used for design implementation.