On the VLSI Energy Complexity of LDPC Decoder Circuits

Abstract:

Sequences of randomly generated bipartite configurations are analyzed; under mild conditions almost surely such configurations have minimum bisection width proportional to the number of vertices. This implies an almost sure $\Omega (n^2/d^2 \text{ max})$ scaling rule for the energy of directly-implemented LDPC decoder circuits for codes of block length $n$ and maximum node degree $d_{\text{max}}$. It also implies an $\Omega (n^{3/2}/d_{\text{max}})$ lower bound for serialized LDPC decoders. It is also shown that all (as opposed to almost all) capacity-approaching, directly-implemented non-split node LDPC decoding circuits, have energy, per iteration, that scales as $\Omega (x^2 \ln^3 x )$, where $x = (1 - R/C)^{-1}$ is the reciprocal gap to capacity, $R$ is code rate and $C$ is channel capacity.

Existing system

The first result is an “almost-sure” scaling rule for the energy complexity of LDPC decoders. In particular, we analyze ensembles generated according to a uniform configuration distribution. We show, subject to some mild conditions, the minimum bisection width of a randomly-generated bipartite configuration asymptotically almost surely has minimum bisection width proportional to the number of vertices. This implies an $\Omega (n^2=d^2_{\text{max}})$ lower bound on the energy of directly-implemented LDPC decoders and a $\Omega (n^3=2=d_{\text{max}})$ lower bound on the energy of serialized decoders.

Proposed system

This uses an adaptation of Thompson’s VLSI model to derive lower bounds on the VLSI energy complexity of low-density parity-check (LDPC) codes, an important family of error control codes.

Applications

1) Communications
2) Digital signal processing

Advantages

Area, delay and power reduced

System Configuration:

In the hardware part a normal computer where Xilinx ISE 14.3 software can be easily operated is required, i.e., with a minimum system configuration

HARDWARE REQUIREMENT

Processor - Pentium –III

Speed - 1.1 GHz

RAM - 1 GB (min)

Hard Disk - 40 GB

Floppy Drive - 1.44 MB

Key Board - Standard Windows Keyboard

Mouse - Two or Three Button Mouse

Monitor - SVGA

SOFTWARE REQUIREMENTS

✧ Front End : Modelsim 6.3 for Debugging and Xilinx 14.3 for Synthesis and Hardware Implementation

This software’s where Verilog source code can be used for design implementation.