Near-Threshold RISC-V Core with DSP Extensions for Scalable IoT Endpoint Devices

Abstract:

Endpoint devices for Internet-of-Things not only need to work under extremely tight power envelope of a few milliwatts, but also need to be flexible in their computing capabilities, from a few kOPS to GOPS. Near-threshold (NT) operation can achieve higher energy efficiency, and the performance scalability can be gained through parallelism. In this paper, we describe the design of an open-source RISC-V processor core specifically designed for NT operation in tightly coupled multicore clusters. We introduce instruction extensions and microarchitectural optimizations to increase the computational density and to minimize the pressure toward the shared-memory hierarchy. For typical data-intensive sensor processing workloads, the proposed core is, on average, 3.5× faster and 3.2× more energy efficient, thanks to a smart L0 buffer to reduce cache access contentions and support for compressed instructions. Single Instruction Multiple Data extensions, such as dot products, and a built-in L0 storage further reduce the shared-memory accesses by 8× reducing contentions by 3.2×. With four NT-optimized cores, the cluster is operational from 0.6 to 1.2 V, achieving a peak efficiency of 67 MOPS/mW in a low-cost.

Existing system

We have been exposed to an increasing demand for small, and battery-powered Internet-of-Things (IoT) endpoint devices that are controlled by a microcontroller (MCU), interact with the environment, and communicate over a low-power wireless channel. It is expected that the demand for sensors and processing platforms in the IoT segment will skyrocket over the next years. Current IoT endpoint devices integrate multiple sensors, allowing for sensor fusion, and are built around an MCU, which is mainly used for controlling and lightweight processing. Since endpoint devices are often untethered, they must be very inexpensive to maintain and operate, which requires ULP operation. As the power of wireless (and wired) communication...
from the endpoint to the higher level nodes in the IoT hierarchy is still dominating the overall power budget. A simple MCU is very efficient for controlling purposes and lightweight processing, but not powerful nor efficient enough to run more complex algorithms on parallel sensor data streams.

**Proposed system**

We focus on building a microarchitecture based on the RISC-V ISA, which achieves similar performance and code density to the state-of-the-art MCUs based on a proprietary ISA, such as ARM Cortex-M series cores. The focus is on ISA and microarchitecture optimization, specifically targeting NT parallel operation, when cores are embedded in a tightly coupled shared-memory cluster. The back-end of the RISC-VGCC compiler has been extended with fixed-point support, hardware loops, postincrement addressing modes, and SIMD instructions.

**Applications**

1) Communications
2) Digital signal processing

**Advantages**

Area, delay and power reduced

**System Configuration:**

In the hardware part a normal computer where Xilinx ISE 14.3 software can be easily operated is required, i.e., with a minimum system configuration.

**HARDWARE REQUIREMENT**

Processor - Pentium –III
Speed - 1.1 GHz

RAM - 1 GB (min)

Hard Disk - 40 GB

Floppy Drive - 1.44 MB

Key Board - Standard Windows Keyboard

Mouse - Two or Three Button Mouse

Monitor - SVGA

SOFTWARE REQUIREMENTS


❖ Front End : Modelsim 6.3 for Debugging and Xilinx 14.3 for Synthesis and HardWare Implementation

This software’s where Verilog source code can be used for design implementation.