A Scalable Network-on-Chip Microprocessor with 2.5 D Integrated Memories and Accelerator

Abstract:

A 2.5D integrated microprocessor die, memory die, and accelerator die with 2.5D silicon interposer I/Os. The use of such 2.5D silicon interposer I/Os provide a scalable interconnection for core-core (up to 32 cores), core-memory (4× storage capacity) and core accelerator (4.4× speedup in H.264 decoder). The 2.5D integrated chip was implemented in GF 65 nm process with multicore microprocessor operated at 500 MHz under 1.2 V supply with 1.08 W power dissipation. A pair of 8 Gbps 2.5D silicon interposer I/O is designed for each of 12 inter-die communication channels, achieving a bandwidth of 24 GBps with 7.5 pJ/bit energy efficiency. As a result, the specified applications such as H.264 video data analytics and AES encryption can achieve significant performance improvement of throughput and energy efficiency.

Existing system

The advance technology scaling and system integration, a large number of processing cores can be progressively integrated for high throughput, but is difficult to maintain a low power density. Heterogeneous multicore microprocessors are normally integrated with dedicated accelerators for application specified computing. With further integration of memory, one can develop energy efficient computing platform to support future data-oriented analytics for servers and also edge devices. The traditional 2D integration suffers from low efficiency, delay, high power and also area as the I/O interconnect between logic and memory started to dominate the system performance. The 3D integration, performed by vertical stacking of dies using through-silicon vias (TSVs), enjoys the benefit of high efficiency of logic memory integration. However, thermal dissipation becomes the major concern in the 3D integration. On the other hand, 2.5D integration, in which multiple dies are placed on one common substrate and are connected using silicon interposers, are designed as medium-distance transmission lines (T-lines) for logic and memory integration.
Proposed system

We further fabricate the through silicon interposer with all dies integrated. The entire chip was implemented in GF 65 nm process. The multicore microprocessor operates at 500 MHz under 1.2 V supply with 1.08 W power dissipation. The 2.5D silicon interposer based I/Os support 12-way full-duplex communication in parallel, bringing the bandwidth up to 24 GB/s with 7.5 pJ/bit energy efficiency. A functional level system partitioning strategy is followed here, targeting scalable future data-oriented computing systems. A functional level partitioning in such 2.5D or 3D systems yield significant benefits without large partitioning overhead.

Applications

1) Communications
2) Digital signal processing

Advantages

Area, delay and power reduced

System Configuration:-

In the hardware part a normal computer where Xilinx ISE 14.3 software can be easily operated is required, i.e., with a minimum system configuration

HARDWARE REQUIREMENT

<table>
<thead>
<tr>
<th>Processor</th>
<th>- Pentium –III</th>
</tr>
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<tbody>
<tr>
<td>Speed</td>
<td>- 1.1 GHz</td>
</tr>
<tr>
<td>RAM</td>
<td>- 1 GB (min)</td>
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<tr>
<td>Hard Disk</td>
<td>- 40 GB</td>
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</tbody>
</table>
SOFTWARE REQUIREMENTS


❖ Front End : Modelsim 6.3 for Debugging and Xilinx 14.3 for Synthesis and Hard Ware Implementation

This software’s where Verilog source code can be used for design implementation.